

# The Design of Bit-Serial Lattice Wave Digital Filter Using FPGA

Warin Sootkaneung

Department of Electrical Engineering  
Rajamangala University of Technology Phra Nakhon, Thewes Campus  
Bangkok, Thailand

**Abstract**—This article describes an efficient approach to the implementation of bit-serial lattice wave digital filters based on field programmable gate array (FPGA). In this paper, a time schedule of all of the bit-serial two-port adaptors is presented as a bridge between conception and completion. Finally, with the satisfying frequency response, the filter is successfully tested by both computer simulation and real signal measured from the programmed FPGA.

**Keywords**—lattice wave digital filters, bit-serial, two-port adaptors, field programmable gate array (FPGA)

## I. INTRODUCTION

The wave digital filter is one of the structures of the infinite impulse response (IIR) digital filter. By using an analog filter as the prototype circuit, either voltage or current variables in the analog circuit are completely changed into wave variables: incident and reflected waves [1]. Due to being low sensitivity in analog networks, we can also reduce the coefficient word length of the digital filter. As a result, the wave digital filters directly benefit the period of multiplication as well as the area consumption within the chip. This kind of digital filter becomes more popular to be implemented into many varieties of integrated circuits.

The lattice wave digital filter can be derived from an analog lattice-LC circuit in which its sensitivity is naturally a bit lower in the passband than in the stopband. Nevertheless, there is less number of coefficients in the analog lattice-LC than in the LC-ladder network, having very low sensitivity, and the structure of the lattice wave digital filter is very simple so it is very famous one [2].

This paper illustrates the design steps of the bit-serial lattice wave digital filter by presenting a technique for multiplexing the processing elements in the time schedule pattern and a method for real circuit design. Lastly, the whole algorithm is programmed into a Xilinx FPGA that is later tested for its frequency responses.

## II. LATTICE WAVE DIGITAL FILTER

The structure illustrated in Figure 1 will be called the two-port adaptor. For each  $n$  two-port adaptor,  $x_n$  and  $v_n$  are the variables of incident waves, and  $y_n$  and  $u_n$  are the variables of reflected wave.

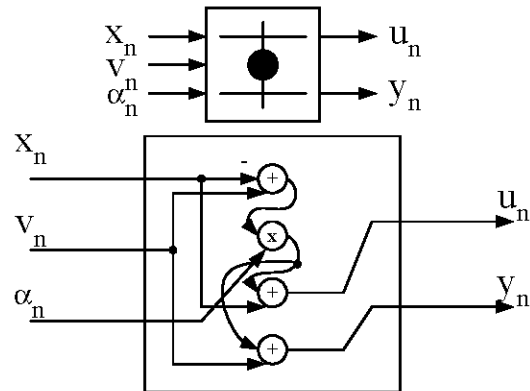


Figure 1. Structure of the two-port adaptor

The relations between these variables are obtained as follows,

$$y_n = v_n + \alpha_n (u_n - x_n) \quad (1)$$

and

$$u_n = x_n + \alpha_n (v_n - x_n) \quad (2)$$

where  $\alpha_n$  is coefficient of each two-port adaptor.

According to those equations, if  $u_n$  and  $v_n$  are connected together via a delay element ( $T$ ) shown in Figure 2(a), This will be called the 1<sup>st</sup>-order allpass filter and its transfer function in  $z$ -domain becomes

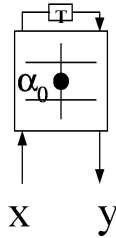
$$G_1(z) = \frac{y_n}{x_n} = \frac{-\alpha_0 + z^{-1}}{1 - \alpha_0 z^{-1}}, \quad (3)$$

where  $\alpha_0$  is the coefficient of the 1<sup>st</sup>-order allpass filter.

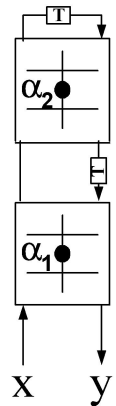
If we consider Figure 2(b) carefully, we will have the transfer function of the 2<sup>nd</sup>-order allpass filter. That is

$$G_2(z) = \frac{-\alpha_1 + \alpha_2(\alpha_1 - 1)z^{-1} + z^{-2}}{1 + \alpha_2(\alpha_1 - 1)z^{-1} - \alpha_1 z^{-2}}, \quad (4)$$

where  $\alpha_1$  and  $\alpha_2$  are coefficients of the 2<sup>nd</sup>-order allpass filter.



(a)



(b)

Figure 2. 1<sup>st</sup> and 2<sup>nd</sup> allpass filters

The structure of lattice wave digital filter consists of two parallel circuits as show in Figure 3. The transfer function of this circuit is

$$H(z) = \frac{1}{2}(A_1(z) + A_2(z)). \quad (5)$$

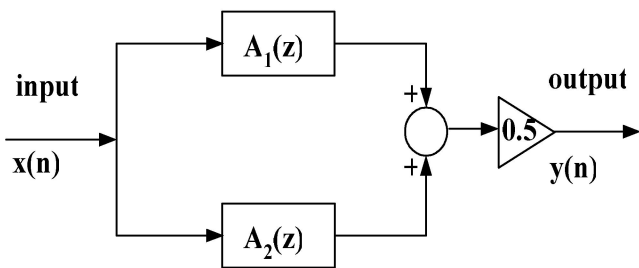


Figure 3. Parallel connection of two circuits

If the order of  $A_1$  and  $A_2$  are considered to be  $m$  and  $n$  respectively, in the case of lowpass filter, the value of  $|m - n|$  is always 1 [3]. The transfer functions which can be rewritten in terms of the coefficients of two-port adaptors are

$$A_1(z) = \frac{-\alpha_0 + z^{-1}}{1 - \alpha_0 z^{-1}} \prod_{i=1}^{(m-1)/2} \frac{-\alpha_{2i-1} + \alpha_{2i}(\alpha_{2i-1} - 1)z^{-1} + z^{-2}}{1 + \alpha_{2i}(\alpha_{2i-1} - 1)z^{-1} - \alpha_{2i-1}z^{-2}} \quad (6)$$

and

$$A_2(z) = \prod_{i=(m+1)/2}^{(m+n-1)/2} \frac{-\alpha_{2i-1} + \alpha_{2i}(\alpha_{2i-1} - 1)z^{-1} + z^{-2}}{1 + \alpha_{2i}(\alpha_{2i-1} - 1)z^{-1} - \alpha_{2i-1}z^{-2}} \quad (7)$$

where  $\alpha_0$  is the coefficient of two-port adaptor belonging to the 1<sup>st</sup>-order polynomial, and  $\alpha_{2i-1}$  and  $\alpha_{2i}$  are the values of the 2<sup>nd</sup>-order polynomial.

### III. FILTER SYSTEM DESIGN

It is desired to design an elliptic lowpass filter with the cut-off frequency at  $0.05f_s$ . The maximum acceptable passband ripple and the required stopband attenuation are 1 dB and 30 dB, respectively, where  $f_s$  is sampling frequency.

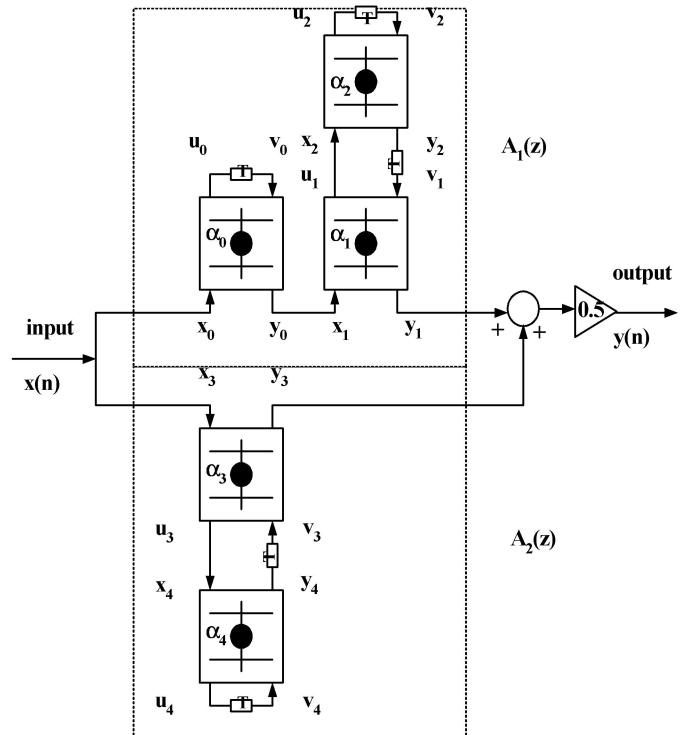


Figure 4. The 5<sup>th</sup>-order lattice wave digital filter

After having been calculated [1], [4], [5], the lattice wave digital filter is fifth-order. Its coefficients after optimization are shown in Table 1. The design is performed by bit-serial processing elements which are represented by the 2's complement number system. The data bits have the word length at 22, and the calculated result gives the optimum coefficient word length at least 9 bits including a sign-extension bit.

TABLE I. THE OPTIMIZED COEFFICIENTS OF THE 5<sup>TH</sup> ORDER LOWPASS FILTER

Coefficients	8-bit word length (Decimal number)	9-bit binary word length (including a sign bit)
$\alpha_0$	0.875	0.11100000
$\alpha_1$	-0.9685	1.00001000
$\alpha_2$	0.9492185	0.11110011
$\alpha_3$	-0.859375	1.00010100
$\alpha_4$	0.96875	0.11111000

In bit-serial arithmetic, the data flows bit by bit through each processing element synchronized by the global internal clock. One group of data uses totally 22 clock cycles to be completely released from the least to the most significant bit so that the period of sampling is equal 22D (D = D-flip flop).

This system uses bit-serial adders which cause the latency at 1 clock cycle. For multiplication, serial/parallel multipliers are applied and will cause a delay of 9 clock cycles depending only on the coefficient word length [6].

After all components in this system have been defined, the time schedule shown in Figure 5, illustrated separately with two sub-circuits:  $A_1$  and  $A_2$ , can be achieved by dividing the time into several intervals. Each is equal one internal clock cycle. There are only three kinds of elements within the schedule: the adders, multipliers and delays. Every processing element and delay characteristic is arranged into the schedule which is connected by the thick lines indicating the number of delay elements. As a matter of fact, the number of intervals passed by those lines is exactly the same as the whole number of delay components in this digital circuit.

Besides, the signals  $v_0(n)$ ,  $v_1(n)$ ,  $v_2(n)$ ,  $v_3(n)$ , and  $v_4(n)$ , which are the outputs of the delay elements (Ts), are fed from the signals  $v_0(n+1)$ ,  $v_1(n+1)$ ,  $v_2(n+1)$ ,  $v_3(n+1)$ , and  $v_4(n+1)$  at the next period (= 22D).

Consequently, the outputs of both  $A_1$  and  $A_2$  circuits have to be summed together at 23D and the summation has to be scaled by a half-multiplier later at 24D, so the final circuit output can be achieved after 25 internal clock cycles has reached.

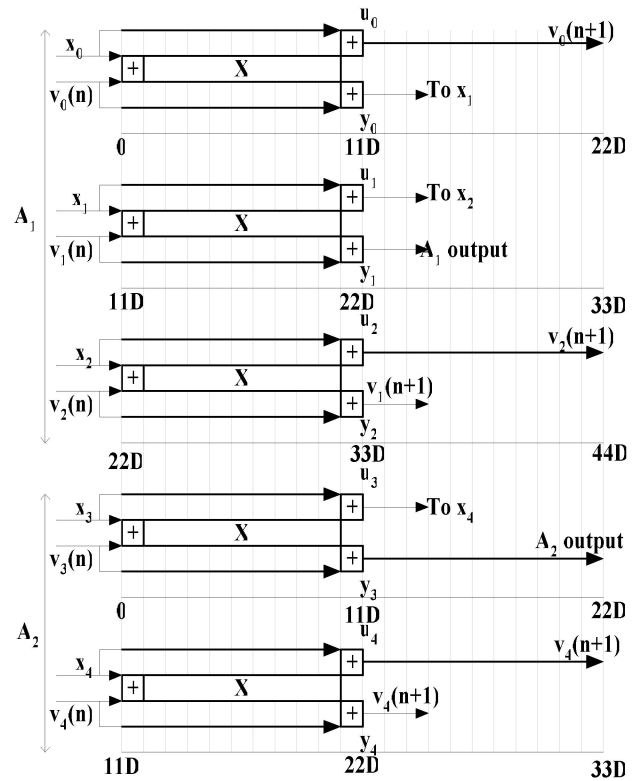


Figure 5. The time schedule of the 5<sup>th</sup>-order lattice wave digital filter

#### IV. FPGA IMPLEMENTATION

In this selective work, the Xilinx Spartan-II FPGA is used to implement our lattice wave digital filter algorithms which have been already designed in previous section. The FPGA is programmed using a combination of Xilinx core generation and hardware description language (HDL) code.

The diagram of this hardware shown in Figure 6 consists of bit-serial two-port adaptors, ROM and its counter, control circuit and post processing elements (the last adder and half-multiplier).

The input signals are the serial input  $x$  and *Global CLOCK*. In this bit-serial system, the clock signal is the most important thing used to synchronize all of the bit-serial processors and trigger all of the control circuits as well.

Both  $A_1\_OUT$  and  $A_2\_OUT$  are the output signals of each parallel circuit. These outputs will have to be added together and then the solution is multiplied by 0.5 therefore the total output  $y$  will be ultimately achieved.

The ROM in this circuit is responsible for giving 9-bit parallel coefficients out to each serial/parallel multiplier at the exact time provided by the counter.

The XC2S200PQ208 FPGA, composing of 200,000 total equivalent gates, has been selected. After implementation, the circuit carries out a lattice wave digital filter yielding up to 40 MHz for its internal oscillation.

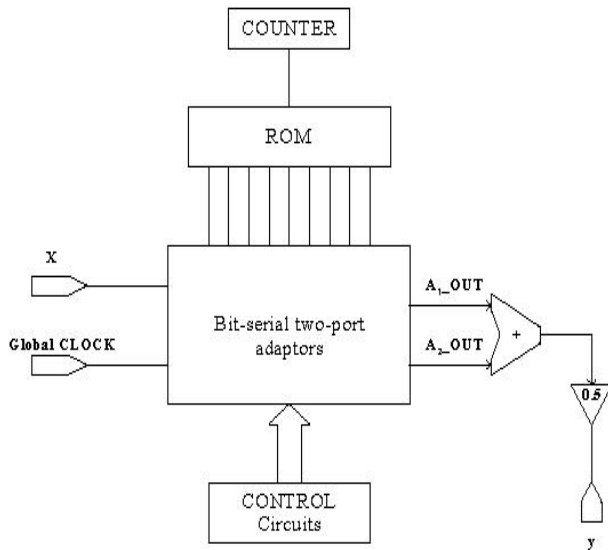
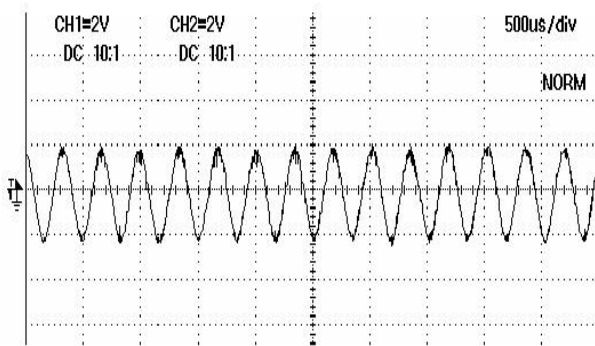
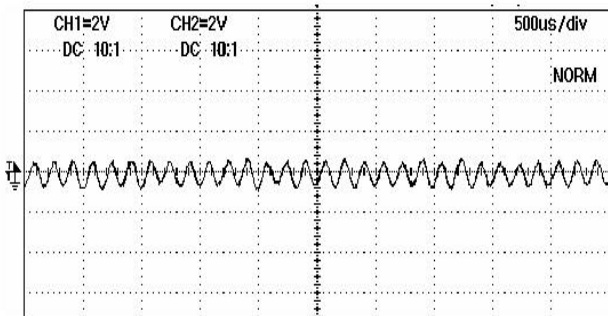


Figure 6. Filter circuit diagram

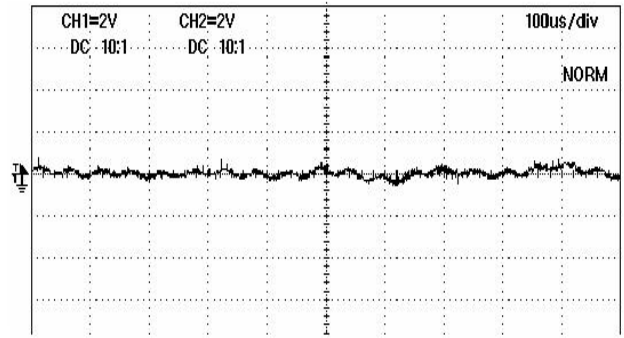
Also, the downloaded FPGA has been tested by real signal at 100 kHz sampling frequency. The time domain responses are shown in Figure 7.



(a) At the frequency below the filter cut-off frequency



(b) At the frequency within the transition band



(c) At the frequency within the stop band

Figure 7. The outputs of lattice wave digital lowpass filter for each frequency band

The circuit frequency responses shown in Figure 8 have been plotted by measuring the magnitude of the response corresponding with each varied input frequency in decibel unit (dB). The horizontal axis indicates the values of normalized frequency.

The computer simulation, having no round-off error, drawn by the thick line is also illustrated to compare the result to the real frequency response (star-line) which has the effect of round-off error.

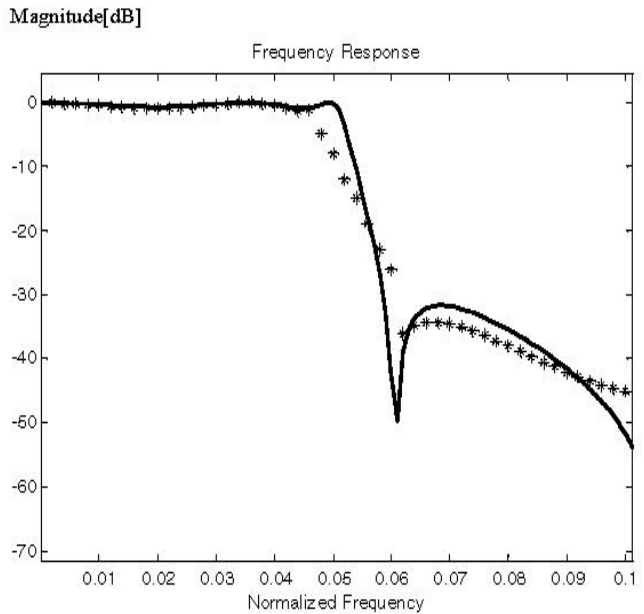


Figure 8. Circuit frequency responses

## V. CONCLUSION

The design of lattice wave digital filter based on field programmable gate arrays (FPGAs) has been clearly proposed. To begin with, the optimized coefficients of our lattice wave digital filter have been acquired as well as simulated for the functional frequency responses.

In gate level, this paper has described the technique for putting down the time schedule configured by bit-serial

processing elements. Afterwards, this time schedule has been successfully mapped and implemented into the Xilinx Spartan-II FPGA (XC2S200), and so we accomplish the 5<sup>th</sup>-order lattice wave digital filter with the maximum internal clock frequency at about 40 MHz. With the satisfying results, the responses have been also consolidated by measuring the real output signal.

#### REFERENCES

- [1] S. Lawson and A. Mirzai, *Wave Digital Filters*, Ellis Horwood, New York, 1990.
- [2] S. Lawson, "Wave Digital Filters Boost DSP Applications," *IEEE Circuits and Devices Magazine* vol.84, pp. 27-31, 1992.
- [3] J. Yli-Kaakinen and T. Saramaki, "An efficient algorithm for the design of lattice wave digital filters with short coefficient wordlength," *IEEE International Symposium on Circuit and System* vol.3, pp. 443-448, 1999.
- [4] V. K. Ingle and John G. Proakis, *Digital Signal Processing Using MATLAB V.4*, PWS-ITP, Boston, 1997.
- [5] A. Antoniou, *Digital filters: Analysis, Design and application*, 2<sup>nd</sup>ED, Mcgraw-Hill, New York, 1993.
- [6] L. Wanhammar, *DSP Integrated Circuit*, Academic Press, San Diego, 1999.