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Particle Swarm Optimization Based NBTI Modeling for FinFET Circuits

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Received 13 October 2016; accepted 13 March 2017

Abstract

Fin Field Effect Transistor (FinFET) technology has increasingly been adopted for use within integrated circuits thanks to its superior electrical integrity and scalability. However, a steady increase in vulnerability of FinFET circuits to negative bias temperature instability (NBTI) has recently become one of the major lifetime reliability problems. In this paper, we propose a simulation framework to address NBTI in combinational circuits implemented with 14-nm tri-gate FinFET predictive technology. Particle swarm optimization (PSO) algorithm is applied to construct an accurate long-term NBTI degradation model from cycle-by-cycle data history. The proposed simulation methodology provides accurate results with high efficacy in computation time compared to reference models. From the proposed framework, the average delay degradation for all experimental circuits under normal operation after 10-year NBTI stress is approximately 6%, yet temperature variation in the circuit strongly influences NBTI degradation.

Keywords: Delay; FinFET; Negative Bias Temperature Instability (NBTI); Particle Swarm Optimization (PSO); Threshold Voltage; Workload

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1. Introduction

NBTI is a temporal mechanism that causes a shift in threshold voltage (V_{th}) in a P-channel device when receiving negative input. The shift in threshold voltage consequently causes poorer delay performance. Because of FinFET's non-planar structure, FinFETs expand NBTI reaction area [1] and raise the self-heating effect that worsens NBTI degradation due to increased temperature [2]. For FinFET based SRAMs, some techniques have lately been proposed to address NBTI as well as to improve SRAM reliability against NBTI [3], [4], [5]. On the other hand, there have also been other recent efforts to develop aging models for NBTI degradation in FinFET logic circuits as follows. The study in [6] introduces a unified model for both NBTI and Hot Carrier Injection (HCL) to predict the circuit lifetime. The work in [7] models the reliability of FinFET standard cells considering NBTI and process variation for future technology nodes. The investigation in [8] explores the delay effects and frequency dependence of NBTI in high-k/metal gate FinFET logic circuits. Analysis of NBTI in datapath logic subblocks at netlist level in [9] reveals that the correlation of NBTI aging sensitivity to workload variations and architectural parameters is remarkably high. Among recent studies on NBTI, few of those comprehensively take into account the arbitrary bias level that profoundly affects NBTI stress. For this reason, most recent NBTI models tend to yield overestimated results.

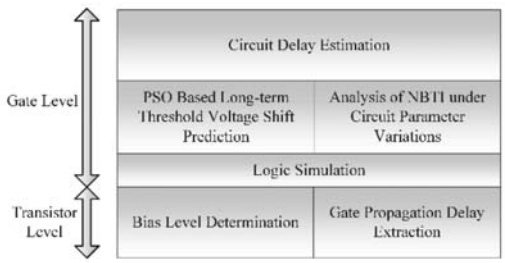

Fig. 1. NBTI simulation and analysis framework

To improve accuracy and scalability in NBTI prediction, we introduce a simulation framework for addressing NBTI in FinFET combinational circuits. In this framework, particle swarm optimization (PSO) algorithm is applied to construct a long-term threshold voltage shift model from cycle-by-cycle NBTI degradation history. PSO developed by Kennedy and Eberhart [10] imitates social behavior of animal in a moving swarm where each population member (or the so-called "particle") can evolutionarily achieve better position based on its knowledge learned from its own and from neighbor experiences. Since PSO algorithm is easy to implement and fast to converge, we select this evolutionary algorithm to fit the parameters in our proposed long-term NBTI model by means of solving a nonlinear fitting problem. The main contribution of this study is to predict long-term NBTI degradation that

includes arbitrary bias and temperature levels on individual transistors. The framework shown in Fig. 1 covers hierarchical NBTI modeling and analysis from transistor level to gate level of the design. At the transistor level, we perform extensive simulation to obtain bias voltage and propagation delay profiles for all gates in our design library. Logic simulation, PSO based long-term threshold voltage shift calculation, and circuit delay determination are performed at the gate level. We apply the proposed NBTI model to a number of experimental circuits to explore long-term circuit delay degradation under temperature variation. The rest of the paper is organized as follows. Sections 1.1 and 1.2 provide important background of NBTI and PSO algorithm, respectively. The proposed long-term NBTI modeling is introduced in Section 2. Section 3 discusses experimental results and we finally conclude the study in Section 4.

1.1 Dynamic NBTI Model

NBTI effect can be described by the Reaction-Diffusion (R-D) theory [11], [12]. The reaction starts at the Si/SiO_2 interface of a negatively biased P-channel transistor. There are some broken Si-H bonds at the interface as a result of holes from the inversion layer tunneling into the gate oxide. This reaction (or the so-called "stress phase") generates incomplete Si^+ bonds at the interface (interface traps) and releases H atoms diffusing away from the interface. When the negative bias is removed, some of the hydrogen species diffuse back and repassivate the broken Si^+ bonds. Fast recovery takes effect first from the H_2 in the oxide which can quickly anneal the interface traps. A subsequent recovery (slow recovery) then takes place from the H_2 in Poly-Si diffusing back to the interface.

Consider 1-D diffusion to simplify the complication of geometry dependence. The dynamic model for threshold voltage shift (ΔV_{th}) covering both stress and recovery phases can be obtained [3]:

Stress:

$$\Delta V_{th}(t) = \left[K_v (t - t_0)^{\frac{1}{2}} + \sqrt[2n]{\Delta V_{th}(t_0)} \right]^{2n} \quad (1)$$

Rec.:

$$\Delta V_{th}(t) = \Delta V_{th}(t_1)\left(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(t - t_1)}}{2t_{ox} + \sqrt{C\,t}}\right) \quad (2)$$

Where C is the diffusion temperature-dependent coefficient; n is set to be 1/4 or 1/6 for H diffusion or H_2 diffusion, respectively [13]; the times t_0 and t_1 correspond to the time at the beginning of stress phase and recovery phase, respectively; ξ_1 and ξ_2 are constants; t_e is the effective diffusion distance; t_{ox} is the oxide thickness; and the term K_v is given by

$$K_v = \left(\frac{q\,t_{ox}}{E_{ox}}\right)^3 \cdot K_1^{\,2} C_{ox}(V_{gs} - V_{th})\sqrt{C}\ exp\left(\frac{2E_{ox}}{E_0}\right) \quad (3)$$

where E_{ox} is the vertical electric field, E_0 is a technology dependent parameter, K_1 is a constant, and V_{gs} is the gate-source voltage of the device.

1.2 Particle Swarm Optimization (PSO)

Particle swarm optimization (PSO) is one of the evolutionary computation methods to search for potential solutions based on swarm intelligence of insects, birds, or fish. In PSO, an individual or particle is represented by its position and velocity which indicate a possible solution and search direction, respectively. All particles iteratively evaluate their move and update the position and velocity based on their own and group's (swarm's) experiences. The position and velocity vectors of the *i*-th particle in the *d*-dimensional search space are represented as $\mathbf{P_i} = [p_{i,1}, p_{i,2}, p_{i,3},\ldots, p_{i,d}]^T$ and $\mathbf{V_i} = [v_{i,1}, v_{i,2}, v_{i,3},\ldots, v_{i,d}]^T$, respectively. Each particle has its own personal best position, $\mathbf{P_i^b} = [p_{i,1}^b, p_{i,2}^b, p_{i,3}^b,..., p_{i,d}^b]^T$, achieved so far at the end of *j*-iteration. In the entire swarm, the best of the personal best position found so far is represented as the global best position, $\mathbf{P^g} = [p_1^g, p_2^g, p_3^g,.., p_d^g]^T$. At the (*j*+1)-iteration, the particle velocity, $\mathbf{V_i^{j+1}}$, and position, $\mathbf{P_i^{j+1}}$, are updated according to the evolution equations [14] as follows.

$$\mathbf{V_i^{j+1}} = \omega * \mathbf{V_i^j} + c_1 * r_1 * (\mathbf{P^g} - \mathbf{P_i^j}) + c_1 * r_2 * (\mathbf{P_i^b} - \mathbf{P_i^j}) \quad (4)$$

$$\mathbf{P_i^{j+1}} = \mathbf{P_i^j} - \mathbf{V_i^j} \quad (5)$$

In (4) and (5), ω is the inertia weight, c_1 and c_2 are the learning factors, and r_1 and r_2 are random numbers in [0, 1].

2. Research Methodology

2.1 PSO Based NBTI Prediction

In this study, PSO algorithm is used to construct a long-term NBTI model guided by the dynamic degradation in (1), (2), and (3). Since a PFinFET receives arbitrary stress level and time duration depending on its V_{gs} for each cycle, the results from the dynamic model are recorded as degradation history that helps capture stress-recovery behavior of the device under actual operation. The long-term NBTI degradation at the time *t* in a PFinFET can reasonably be considered as power law degradation:

$$\Delta V_{th,long}(t) = K_c * t^{Ke} \quad (6)$$

where K_c and K_e are constants which are dependent on various operating parameters such as supply voltage, temperature, probability of stress, input cycle time, and device geometrical parameters.

A nonlinear problem is formulated to fit the input-dependent constants, K_c and K_e, in (6). The objective is to minimize the sum of square error (*SSE*) between short-term cycle-by-cycle data ($\Delta V_{th,cycle}$) resulted from (1) and (2) and

generated long-term degradation data ($\Delta V_{th,long}$) in (6). The *SSE* can be described as

$$SSE = \sum_{k=1}^{\#\text{of data points}} [\Delta V_{th,cycle}(t_k) - \Delta V_{th,long}(t_k)]^2 \quad (7)$$

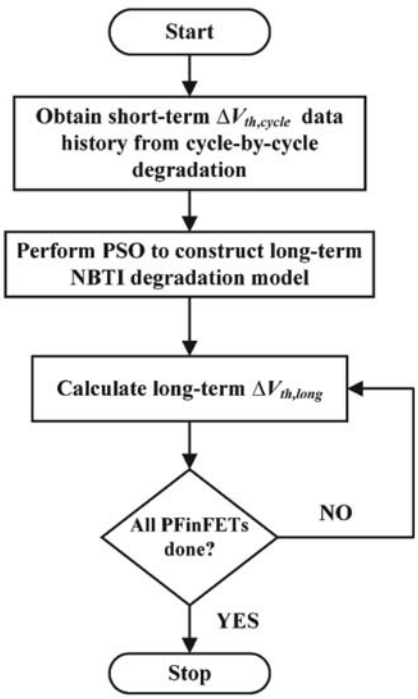

Fig. 2. Flowchart of PSO based long-term NBTI prediction

```
//Initialization
for each particle i = 1 to swarm size do {
    Randomly generate P_i and V_i
     ← P_i
    Save SSE of each
}// end for each particle

Save minimum SSE of the swarm
 ← best {}// with minimum SSE

//Main Loop
for each iteration j = 1 to #of max iteration do {

    //Evaluation
    for each particle i = 1 to swarm size do {
        if (SSE of P_i < SSE of )then {
                ← P_i
            Save SSE of current
        }
        if (SSE of < SSE of )then {
                ←
            Save minimum SSE
        }
    }// end for each particle

    //Update
    for each particle i = 1 to swarm size do {
        V_i ← ω*V_i + c_1*r_1*(P_i) + c_2*r_2* (P_i)
        P_i ← P_i + V_i
    }//end for each particle

}//end for each iteration
```

Fig. 3. Pseudocode of PSO algorithm in long-term NBTI prediction model

In summary, the nonlinear fitting problem used for constructing the long-term threshold voltage degradation model due to NBTI can be stated as

Fit : Ke, Ke
Min : SSE (8)

Next, we employ PSO to solve the above nonlinear problem. In this study, the generated values for each particle i,$K_{c,i}$ and $K_{e,i}$, associated with the fitting constants, K_c and K_e , are described as the position of a 2-dimensional particle

(d = 2), and thus, $\mathbf{P_i} = [K_{c,i}, K_{e,i}]^T$, Flowchart of our proposed PSO based long-term NBTI prediction is shown in Fig. 2. The cycle-by-cycle NBTI degradation history ($\Delta V_{th,cycle}$) from (1) and (2) is pre-calculated to determine the *SSE*, the objective function of the problem. Afterwards, we use PSO algorithm to fit the constants, K_c and K_e, of each transistor. Fig. 3 sketches the pseudocode of PSO algorithm applied to this problem. To begin with, the position and velocity vectors, $\mathbf{P_i}$ and $\mathbf{V_i}$, are initialized with random values. Because there is no previous $\mathbf{P_i}$ value for comparison in this initialization stage, the personal best position of the *i*-th particle, $\mathbf{P_i^b}$ is set to be the same as $\mathbf{P_i}$. In the main loop of PSO algorithm, the current particle position, $\mathbf{P_i}$, is evaluated and compared with the previous personal best position, $\mathbf{P_i^b}$, and the global best position, $\mathbf{P^g}$ If the current $\mathbf{P_i}$ provides smaller *SSE*, it will replace $\mathbf{P_i^b}$ or both $\mathbf{P_i^b}$ and $\mathbf{P^g}$. At the end of the main loop, the particle velocity, $\mathbf{V_i}$, and position, $\mathbf{P_i}$, are updated according to the evolution equations, and set to be the velocity and position of the corresponding particle for the next iteration.

2.2 Propagation Delay Model

As we strictly take into account the strong input-dependence of NBTI in this study, each PFinFET in a gate receives different threshold voltage shift. Estimating circuit timing performance requires a propagation delay model that can cope with this unequal threshold voltage degradation among pull-up transistors.

First of all, we assume that all PFinFETs have original threshold voltage of v_{tp0} and rising propagation delay of t_{pdr0}. This t_{pdr0} of a gate has a linear relationship with the load capacitance. Since in this model, the size of both PFinFET and NFinFET with one fin and single finger is considered to be identical, the load capacitance can be reasonably considered linear with the total number of fins ($NFIN_L$) of PFinFETs and NFinFETs connected to the output of the gate. Hence, if all devices have the same number of fingers, we can consider that t_{pdr0} has linear relation with $NFIN_L$ as given below.

$$t_{pdr0} = A NFIN_L + B \quad (9)$$

where ${}_L NFIN$ is the total number of fins of the gate fanout. The constants, *A* and *B*, depend on the gate type and can be identified by linear fitting. Fig. 4 plots t_{pdr0} of various gates versus ${}_L NFIN$ when their load is an inverter with varying size. In this figure, we can see the nearly linear relationship between t_{pdr0} and ${}_L NFIN$. These plots are used to fit all constants in (9) for all of the gates in the design library.

For a series of PFinFET, suppose that $t_{pdr0,i}$ is a component of original delay corresponding to PFinFET M_i where. $t_{pdr0} = \Sigma_i t_{pdr0,i}$. For small change in the

threshold voltage of PFinFET M_i from v_{tp0} to $v_{tp0} + \Delta v_{tp,i}$ that causes the component of original delay corresponding to PFinFET M_i to change from ${}_{i,0pdr}t$ to ${}_{i,0pdr}t + \Delta_{i,pdr}t$ another form of the Elmore delay [15], [16] can be expressed as

$$\Delta t_{pdr,i} = \frac{\alpha \Delta v_{tp,i}}{v_{dd} - v_{tp0}} t_{pdr0,i} \quad (10)$$

Where $\Delta t_{pdr,i}$ is the change in rising propagation delay component corresponding to PFinFET M_i as a result of the shift in threshold voltage $\Delta v_{tp,i}$ for this device.

For Inverter and NAND cases, the maximum change in rising propagation delay, $\Delta t_{pdr,max}$, takes place when only one parallel PFinFET with the largest threshold voltage degradation, $\Delta v_{tp,max}$, turns on. It can be noticed from the relationship in (10) that $\Delta t_{pdr,i}$ is proportional to $\Delta v_{tp,i}$; i.e., for an Inverter or NAND gate,

$$\Delta t_{pdr,max} = C_1 . t_{pdr0} . \Delta v_{tp,max} \quad (11)$$

where t_{pdr0} can be obtained from (9) and the proportional constant C_1 of each gate can be identified by the linear relationship at any fixed value of load capacitance.

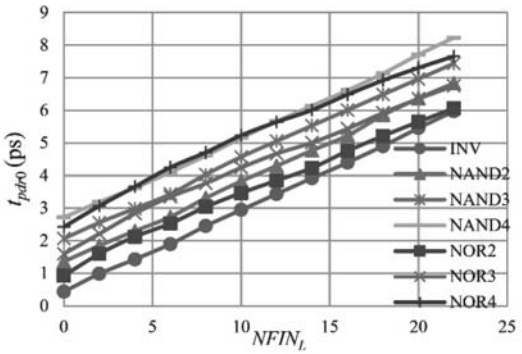

Fig. 4. Original rising propagation delay for different load capacitance

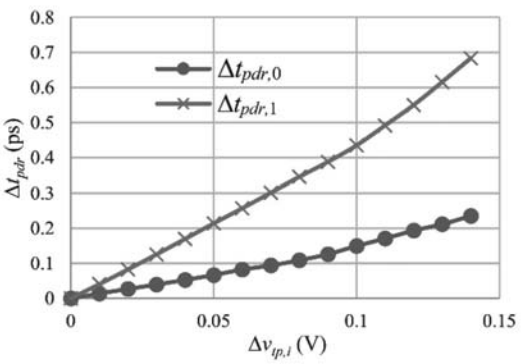

Fig. 5. Change in rising propagation delay in a 2-input NOR gate as a result of threshold voltage shift in each PFinFET

For a NOR gate, the degradation of each PFinFET in series involves in Δt_{pdr} of the gate. In this case, we consider that the component $\Delta t_{pdr0,i}$ also has linear relationship with intrinsic and load capacitance corresponding to PFinFET M_i in series as expressed in the following equation.

$$t_{pdr0,i} = a_i NFIN_L + b_i \quad (12)$$

Where a_i and b_i are parameters of the changes in load capacitance and intrinsic capacitance, respectively. For any NOR gate, $\Sigma a_i = A$ and $\Sigma b_i = B$, where A and B are previously defined in (9). Together with (10) and (12), the change in rising propagation delay of the NOR gate as a result of the shift in threshold voltage in PFinFET M_i can be obtained as follow.

$$\Delta t_{pdr,i} = C_2 .(a_i NFIN_L + b_i).\Delta v_{tp,i} \quad (13)$$

where the gate constant C_2 and transistor constants, a_i and b_i, can be identified by the linear relationship between $\Delta v_{tp,i}$ and $\Delta t_{pdr,i}$ under no load ($NFIN_L$=0) and a fixed value of load capacitance. Fig. 5 shows the change in rising propagation delay of a 2-input NOR gate with $NFIN_L = 8$ when each of the PFinFET M_0 and PFinFET M_1 receives threshold voltage degradation (but not at the same time) and causes the changes in rising delay, $\Delta t_{pdr,0}$ and $\Delta t_{pdr,1}$, respectively. It can be seen that the plots in Fig. 5 underscore the linear expression in (13) for small amount of threshold voltage shift.

Since the total rising propagation delay of a gate, t_{pdr}, is equal to the original rising propagation delay added by the change due to threshold voltage degradation, the rising propagation delay can be stated as

$$t_{pdr} = t_{pdr0} + \begin{cases} \sum_{i=0}^{\#\,of\ inputs-1} \Delta t_{pdr,i}, & for\ NORs \\ \Delta t_{pdr,\max}, & for\ NANDs / INVs \end{cases} \quad (14)$$

Table 1 Maximum threshold voltage degradation in each mapping gate by the end of 10^4-s stress with 10^3-Hz input frequency and 125 °C operating temperature

Gate	Maximum ΔV_{th} (mV)											
	M_0			M_1			M_2			M_3		
	Cycle-by-cycle	*Long-term*	*% Diff*	*Cycle-by-cycle*	*Long-term*	*% Diff*	*Cycle-by-cycle*	*Long-term*	*% Diff*	*Cycle-by-cycle*	*Long-term*	*% Diff*
INV	48.61	49.83	2.51	-	-	-	-	-	-	-	-	-
NOR2	48.61	49.83	2.51	42.01	42.91	2.14	-	-	-	-	-	-
NOR3	48.61	49.83	2.51	44.52	46.11	3.57	39.39	40.24	2.16	-	-	-
NOR4	48.61	49.83	2.51	46.91	49.02	4.50	43.14	44.22	2.50	28.50	29.00	1.72

3. Experimental Results

This section gives experimental results and discusses some interesting remarks found in this study. Our gate-level simulation framework is implemented in JAVA on a 2.50-GHz Intel Core i7 machine with 16-GB memory. A number of experimental circuits selected from the ISCAS-85 suite are mapped with the cell library that consists of Inverter, and 2- to 4-input NAND and NOR gates. We use predictive 14-nm tri-gate FinFET technology from [17] throughout the experiment. At normal operating condition (without any variation), we set V_{dd} = 0.8 V and the probability of input logic "0" = 0.5 for all primary inputs.

3.1 Model Verification

We verify the proposed long-term threshold voltage shift model by comparing the results of maximum threshold voltage degradation under 10^4-second stress with those from the cycle-by-cycle based approaches as reported in Table 1. In cycle-by-cycle based NBTI prediction, equally weighted 1-kHz inputs are provided to each gate under 125 °C operating temperature and hence, this approach requires 10^7 cycles to complete the task. We perform the proposed long-term PSO based NBTI prediction with 20 particles, 100 iterations, and 1000 data points from cycle-by-cycle based calculation history. For all gates, PFinFET M_0 is connected to the power supply followed by M_1, M_2, and M_3. It can be seen in Table 1 that our proposed PSO based NBTI model yields satisfactory results compared to the referenced cycle-by-cycle based model. Our model provides percent difference bounded within 4.5% while requiring extremely small computation time compared to the cycle-by-cycle based approach.

When the inputs of each gate receive the same probability of logic "0" as set in this experiment, all PFinFETs in NAND gates do not experience the stacking effect, and as a result, all of them degrade equally with the same maximum value as found in the Inverter. For many other NBTI models that consider only one stress level in NOR gates (whenever each of the PFinFETs see the input logic "0", it is always considered to be fully stressed with the maximum V_{gs}), the threshold voltage shift in all PFinFETs in the NOR gates is also considered to be the largest. However, in this study which takes into account the input pattern dependence of NBTI stress, the stacking effect can reduce threshold voltage degradation as large as 40% in some PFinFETs in series according to Table 1.

Table 2 Propagation delay model verification

Gate	t_{pdr} (ps) (SPICE)	t_{pdr} (ps) (proposed model)	% Difference
	NFIN$_L$ = 6		
INV	2.0891	2.1213	0.58
NAND2	2.9955	3.0190	0.78
NAND3	3.8194	3.9224	2.70
NAND4	4.5212	4.6646	3.17
NOR2	2.7832	2.7211	-2.23
NOR3	3.5693	3.6159	1.31
NOR4	4.5687	4.5793	0.23
	NFIN$_L$ = 8		
INV	2.6708	2.6708	-1.05
NAND2	3.6317	3.6735	1.15
NAND3	4.4332	4.4708	0.85
NAND4	5.1068	5.2282	2.38
NOR2	3.2702	3.2224	-1.46
NOR3	4.1442	4.1367	-0.18
NOR4	5.0459	5.0992	1.06

To verify the propagation delay model, we compare the rising propagation delay resulted from SPICE and our model. According to the threshold voltage shift from cycle-by-cycle calculation in Table 1, the results of gate rising propagation delay for different output loads from SPICE and the proposed model are provided in Table 2. In this experiment, the output of a gate is connected to an Inverter with different size (NFINL = 6 and 8) and each PFinFET in the gate has threshold voltage shift as reported in the first column of each Mi in Table 1. The experimental results in Table 2 demonstrate that our proposed delay model provides accurate outcome with few percent difference varying from 0.2% to 3.2%.

Table 3 10-year delay degradation under temperature variation

Circuit	10-year Delay Degradation (%)		
	48°C	*80°C*	*112°C*
C17	4.62	7.24	9.42
C499	4.14	6.91	8.60
C880	3.86	5.89	8.31
C1196	4.01	6.52	8.47
C1355	5.74	7.34	9.89
C1908	4.25	7.08	9.04
C2670	3.74	5.69	8.16
C5315	3.76	5.75	8.22
C6288	3.59	5.45	8.04
C7552	3.52	5.38	7.97
Average	4.12	6.32	8.61

3.2 Long-Term NBTI Prediction

An analysis of NBTI degradation under temperature variation is performed in this experiment. As temperature reduction by most thermal management techniques is about 30%-45% of the full-load core temperature [18], we consider a set of operating temperature values: {48°C, 80°C, 112°C } where the normal temperature is at 80°C and its 40% lower and higher values are 48°C and 112°C, respectively. Table 3 provides the results of 10-year delay degradation in combinational benchmark circuits under different operating temperatures as

defined above and 1-GHz input frequency. From Table 3, the average delay degradation results for all experimental circuits at 48°C, 80°C, and 112°C after 10-year NBTI stress are 4.1%, 6.3%, and 8.6%, respectively. Generally, most dynamic power management techniques require few amount of V_{dd} alteration and slightly more amount of frequency adjustment. Both adjustments have a small direct impact on NBTI degradation [12]. However, the outcome of temperature reduction plays a more crucial role in NBTI degradation reduction as reported in Table 3.

Table 4 10-year delay degradation for different ratio of standby time to temperature cycle time

Circuit	10-year Delay Degradation (%)			
	$r_{standby}$ =5%	$r_{standby}$ =10%	$r_{standby}$ =20%	$r_{standby}$ = 40%
C17	7.18	7.05	6.78	6.25
C499	6.50	6.37	6.10	5.57
C880	5.56	5.46	5.26	4.87
C1196	6.33	6.21	5.96	5.46
C1355	7.26	7.18	7.02	6.70
C1908	6.87	6.73	6.45	5.89
C2670	5.48	5.39	5.19	4.81
C5315	5.42	5.33	5.14	4.76
C6288	5.09	5.00	4.82	4.47
C7552	5.23	5.14	4.96	4.59
Average	6.09	5.99	5.77	5.34

Essentially, a processor can switch from active mode to standby mode where the time duration of each mode and the cooling efficacy define transient thermal response of the chip [19]. In Table 4, we further investigate the impact of thermal switching behavior on NBTI. This table reports the NBTI-induced delay degradation in experimental benchmark circuits for different thermal profiles after 10-year stress. In the standby mode, the operating temperature is assumed to be 40% of the active mode temperature. We define the ratio of standby time to temperature cycle time ($r_{standby}$) which is similar to the duty cycle of a periodic signal.

In this experiment, the temperature cycle time is set to be 100 ms for all circuits whereas different values of $r_{standby}$ are provided. The results in Table IV show that the average delay degradation improves by 4%, 5%, 9%, and 16% with respect to the degradation at nominal operating temperature, when all experimental circuits have $r_{standby}$ of 5%, 10%, 20%, and 40%, respectively. Since this part of experiments is performed under periodic temperature cycle, this setting may not precisely represent the real circuits which have arbitrary temperature responses. However, the proposed methodology allows us to predict long-term NBTI degradation from the measured core temperature on the fly, regardless of the periodicity of temperature.

4. Conclusion

In this paper, we introduce

a simulation framework to address NBTI in 14-nm Tri-gate FinFET combinational circuits. In the proposed framework, we develop a new long-term threshold voltage shift prediction that comprehensively takes into account the input pattern dependence of NBTI. To obtain accurate and fast NBTI estimation, PSO algorithm is applied to construct the long-term threshold voltage shift model from cycle-by-cycle degradation data history. This proposed PSO based long-term NBTI model can capture arbitrary bias and temperature levels on the fly. We also introduce a propagation delay model that can be used in conjunction with our proposed threshold voltage shift model which provides unbalanced threshold voltage among PFinFETs in the same gate. Both long-term threshold voltage and propagation delay models return impressive results compared to the reference models. The results from the proposed models when applied to various benchmark circuits show that average delay degradation for all experimental circuits with 80°C operating temperature under 10-year NBTI stress is as small as 6%. However, thermal responses in terms of temperature level and time duration have a high impact on NBTI degradation. As a whole, this accurate simulation methodology can be effectively used to manage the aging reliability in modern FinFET designs.

5. Acknowledgment

This work was supported in part by Rajamangala University of Technology Phra Nakhon and the Coordinating Center for Thai Government Science and Technology Scholarship Students, National Science and Technology Development Agency under Project SCH-NR2014-271.

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