ผลกระทบจากเอ็นบีทีไอต่อสมรรถนะของวงจรรวมดิจิทัลที่สร้างด้วยเทคโนโลยีฟินเฟต

Impact of NBTI on digital integrated circuits in FinFET technologies

วรินทร์ สุดคนึง

ศุภชัย หอวิมานพร

ศศิธร ชูแก้ว

งานวิจัยนี้ได้รับทุนอุดหนุนจากงบประมาณรายจ่าย ประจำปีงบประมาณ พ.ศ. 2560

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รายนามคณะผู้วิจัย

1. อาจารย์ ดร.วรินทร์ สุดคนึง

หน่วยงาน คณะวิศวกรรมศาสตร์ มหาวิทยาลัยเทคโนโลยีราชมงคลพระนคร

2. ผู้ช่วยศาสตราจารย์ ดร.ศุภชัย หอวิมานพร

หน่วยงาน คณะครุศาสตร์อุตสาหกรรม มหาวิทยาลัยเทคโนโลยีพระจอมเกล้าพระนครเหนือ

3. อาจารย์ ดร.ศศิธร ชูแก้ว

หน่วยงาน คณะครุศาสตร์อุตสาหกรรม มหาวิทยาลัยเทคโนโลยีพระจอมเกล้าพระนครเหนือ

วันเริ่มต้นโครงการ 1 ตุลาคม 2559

วันสิ้นสุดโครงการ 30 กันยายน 2560

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มหาวิทยาลัยเทคโนโลยีราชมงคลพระนคร

ปี พ.ศ. ที่ได้รับทุน 2559

บทคัดย่อ

ปัญหาความร้อนในวงจรรวมฟินเฟตขนาดใหญ่มากจากกระแสขับและปรากฏการณ์ความร้อนสะสมในตัว (Self-heating effect) ส่งผลกระทบอย่างมากต่อสมรรถนะและความเชื่อถือได้ของวงจร โครงงานวิจัยนี้ทำการประเมินสมรรถนะของวงจรคอมบิเนชั่นที่สร้างด้วยเทคโนโลยีฟินเฟตภายใต้อิทธิพลของบีทีไอและอุณหภูมิที่เปลี่ยนแปลงจากการผันแปรของแรงดันแหล่งจ่ายและความถี่ กรอบงานของการจำลองผลที่ได้นำเสนอนี้นำมาใช้กับวงจรวัดเปรียบเทียบสมรรถนะที่สร้างขึ้นจากเทคโนโลยีฟินเฟตขนาด 14 นาโนมิเตอร์ชนิดไตรเกตบัลค์ ผลการทดลองเปิดเผยให้เห็นว่า เมื่ออุณหภูมิสูงขึ้นเวลาหน่วงของการเสื่อมที่เกิดจากบีทีไอจะเพิ่มมากขึ้น แต่อิทธิพลของสมรรถนะที่เพิ่มขึ้นจากกระแสขับจะส่งผลเหนือกว่า คณะผู้วิจัยได้พิสูจน์ต่อมาว่า การเสื่อมจากบีทีไอขึ้นอยู่กับกำลังแหล่งจ่ายและความถี่ของวงจรผ่านทางผลกระทบด้านความร้อน คณะผู้วิจัยยังได้นำเสนอวิธีการลดกำลังไฟฟ้าด้วยการปรับแรงดันและความถี่แบบพลวัติที่สามารถปรับลดแรงดันของวงจรที่มีความร้อนสูงเพื่อคงสมรรถนะไว้ ผลการทดสอบแสดงให้เห็นว่า กำลังไฟฟ้าผลลัพธ์จากวิธีการนี้จะลดลงมากขึ้นสำหรับวงจรทดลองที่ทำงานที่อุณหภูมิแวดล้อมที่สูงขึ้น (ลดลงได้ถึง 66% สำหรับวงจรทดลองบางวงจรที่ทำงานที่อุณหภูมิสูงกว่าอุณหภูมิแวดล้อมฐาน 20 องศาเซลเซียส) พร้อมกับมีการเสื่อมจากบีทีไอที่ลดลง

คำสำคัญ: การไร้เสถียรภาพจากไบอัสและอุณหภูมิ (บีทีไอ); ฟินเฟต; การลดกำลังไฟฟ้า; การผกผันของผลจากอุณหภูมิ; ผลกระทบด้านความร้อน

Abstract

In FinFET-based VLSI designs, heat issues from increase of driving current with temperature and self-heating effect profoundly influence the circuit performance and reliability. This work evaluates the performance of FinFET-based combinational circuits considering BTI stress and thermal effect of supply voltage and frequency variations. The proposed simulation framework is applied to selected benchmark circuits implemented with the 14-nm tri-gate bulk FinFET technology. The experimental results reveal that as temperature increases, BTI aging delay increasingly worsens, yet it is overridden by performance gain from the increase in driving current. We also prove that BTI degradation is dependent on power supply and frequency through their thermal impacts. Further, we introduce a DVFS based power reduction approach that scales down the supply voltage of hot circuits to maintain the performance. The results show that power reduction yielded from the proposed technique is larger for all circuits working at higher ambient temperature (as large as 66% in some experimental circuits working at 20 °C above the baseline ambient temperature) with a slight decrease in BTI degradation.

Key Words: bias temperature instability (BTI); FinFETs; power reduction; temperature effect inversion (TEI); thermal effect

Contents

บทคัดย่อ iii

Abstract iv

List of Figures vii

List of Tables viii

Chapter 1. Introduction 1

1.1 Research problem 1

1.2 Objectives of the research project 2

1.3 Research contributions 2

1.4 Expected benefits 3

1.5 Scope of research 3

Chapter 2. Related Theories and Works 4

2.1 Temperature effect on circuit performance 4

2.2 Temperature effect on BTI aging 7

2.3 Related works 8

Chapter 3. Research Methodology 10

3.1 Temperature evaluation 10

3.2 NBTI evaluation 13

3.3 BTI estimation 17

3.4 Delay evaluation 18

Chapter 4. Experimental Results 20

4.1 Combined impacts of NBTI and BTI (PSO approach) 20

4.2 Combined impacts of TEI and BTI 22

4.3 Impacts of voltage and frequency 25

Chapter 5. Conclusions 27

Bibliography 28

Appendix: Researcher Short Biographies 32

List of Figures

Figure 1. Leakage current vs. temperature for different supply voltage levels in an inverter designed with 14-nm bulk FinFET technology.....5

Figure 2. Simulation and analysis framework.....10

Figure 3. The equivalent shift in threshold voltage with temperature in the 14-nm bulk tri-gate nFinFET (a) and pFinFET (b) for different V_{gs}.....11

Figure 4. Flowchart of PSO based TEI-aware long-term NBTI prediction.....14

Figure 5. Pseudocode of PSO algorithm for long-term NBTI prediction.....16

Figure 6. Impacts of BTI and TEI on delay performance of the circuit C499.....24

List of Tables

Table 1. $|V_{gs}|$ of pFinFETs in a 3-Input NOR gates 12

Table 2. 10-year Delay under Temperature Variation 21

Table 3. Aging degradation, performance, and power under BTI and TEI after 10-year operation 23

Table 4. 10-year delay degradation for different fractions of time that the circuits are in active mode 25

Table 5. TEI-based supply voltage scaling to reduce power consumption.....26

Chapter 1. Introduction

1.1 Research problem

In the era of 3D transistors, FinFET devices outperform their planar counterparts in electrical integrity and lower leakage power. However, due to the alternative structures and doping procedures, self-heating effect and large increase in driving current with temperature, namely temperature effect inversion (TEI), intensify the chip temperature [1], [2]. Unlike conventional MOSFET designs, FinFET-based circuits tend to run faster at high temperature [2], [3] providing positive feedback of heat in the circuits. Heat issues in FinFET designs strongly influence aging degradation, especially bias temperature instability (BTI) that slows down the transistor over time [4]. BTI is a temporal effect, affecting either pFinFET (called negative BTI or NBTI) or nFinFET (called positive BTI or PBTI), that causes degradation in the device threshold voltage (V_{th}). BTI stress depends upon workload and temperature. Due to heat problems, BTI aging has been considered as one of the primary concerns for most modern processors.

In recent years, various works have studied the impacts of BTI and proposed a number of BTI reduction techniques for FinFET and planar MOSFET circuits. Unfortunately, few of them have taken into account BTI alongside with the thermal effects and the presence of TEI. Besides, as supply voltage and frequency variations from dynamic voltage/frequency scaling (DVFS) has come to be mandatory to control power and temperature of most chips, BTI assessment for DVFS systems requires either accurate temperature estimation or on-chip digital thermal sensors that can track the cycles of operating temperature corresponding to the modes of operation. Hence, combined thermal impacts of voltage, frequency, workload, and ambient temperature must be addressed well to predict temperature-dependent reliability of the circuit precisely.

1.2 Objectives of the research project

1.2.1 to analyze the impact of circuit parameter variations on reliability and performance of FinFET digital circuits

1.2.2 to construct scalable and accurate reliability models for BTI aging at the gate level in the presence of TEI

1.2.3 to propose new techniques for reliability improvement in nanoscale digital circuits

1.3 Research contributions

In this study, we develop a simulation framework for BTI analysis considering the thermals effects in combinational FinFET circuits. To address BTI aging delay, we include TEI-induced performance gain in calculating temperature-induced BTI degradation. The proposed simulation framework is further used to investigate the impact of temperature cycle, corresponding to DVFS modes, on BTI stress. Moreover, we take advantage of performance improvement at high temperature to develop a power management technique that eliminates unnecessary power gain from TEI. This technique scales the supply voltage according to the operating temperature to maintain circuit performance at a given cooler baseline level with maximum frequency. The results show that the proposed method provides impressive power reduction and slight BTI improvement for all experimental circuits running in nominal mode without any performance penalty.

1.4 Expected benefits

1.4.1 Academic and development benefits:

The body of knowledge gained from this research will be transferred to students through classroom teaching/learning activities, and it will lead to new research directions that continue to discover more advanced knowledge. On the other hand, as reliability issues in FinFET circuits have not well been unveiled, the discovery from this research has high impact on integrated circuit design development, especially on product reliability improvement.

1.4.2 Economic benefits:

The main focus of this project is to improve the circuit reliability in an integrated manner at the design time. The proposed techniques for reliability/performance improvement can be adopted for use in actual processor manufacturing process. Product quality improvement, in turn, increases marketing effectiveness in IC design industry. In addition, the customers of VLSI products gain benefits from reliable systems. The increase in chip reliability reduces the maintenance costs due to either long- term or short-term failures.

1.5 Scope of research

1.5.1 Experimental benchmark circuits are designed with 14-nm bulk tri-gate FinFET predictive technology.

1.5.2 Analysis and improvement framework covers the gate level of the design and higher extended from device level simulation.

1.5.3 The framework is implemented with high-level language as a CAD-tool for reliability/performance management

Chapter 2. Related Theories and Works

2.1 Temperature effect on circuit performance

The carrier mobility in device channel generally decreases with temperature due to the ionized impurity and phonon scatterings that are material-dependent [5]. While the heavily doped body is required in planar devices to deal with the short-channel effect, FinFETs can yield excellent channel control with intrinsic body. Mobility degradation in the undoped FinFET's body is quite low compared to the change in threshold voltage as temperature increases. The overriding impact of decreased threshold voltage at high temperature raises the driving current (I_{on}) of the FinFET at all supply voltage levels. This thermal response, which is contrary to what we have experienced in most conventional MOSFET devices, is called as the temperature effect inversion (TEI).

As a result of TEI in FinFETs, the change in temperature can be considered as a cause of threshold voltage shift $\Delta V_{th,TEI}$ that varies the driving current I_{on} [3]. Hence, I_{on} in subthreshold and superthreshold regimes as a function of $\Delta V_{th,TEI}$ when the device temperature changes from nominal temperature T_0 to any temperature T, can be expressed in the following equation:

$$I_{on} = \begin{cases} \mu(T) e^{\frac{V_{gs} - [V_{th}(T_0) + \Delta V_{th,TEI}(T)]}{S(T)}}, subthreshold\ regime \\ \mu(T)\left[V_{gs} - [V_{th}(T_0) + \Delta V_{th,TEI}(T)]\right]^{\beta}, \text{otherwise} \end{cases} \quad (1)$$

where μ, S, V_{th}, and β are the carrier mobility, subthreshold swing, threshold voltage, and velocity saturation effect factor, respectively. All of these parameters are temperature-dependent. The increase in I_{on} due to TEI enhances the circuit performance at high temperature, yet provides a large amount of heat accumulated in the device.

A power/thermal model is required to evaluate the chip temperature. In this model, the change in temperature of a VLSI circuit is identified by solving the following differential equation:

$$P_{circuit} = C_{th}\frac{dT}{dt} + \frac{T - T_{amb}}{R_{th}} \quad (2)$$

where T is the die or operating temperature, T_{amb} is the ambient temperature, C_{th} is the thermal capacitance, R_{th} is the thermal resistance, and $P_{circuit}$ is the summation of static and dynamic power components. The steady-state condition requires the term $C_{th}\frac{dT}{dt}$ to be zero; i.e., we have $P_{circuit} = \frac{T - T_{amb}}{R_{th}}$. To find the steady-state temperature, a point of intersection between the plots of $P_{circuit}$ (T) and $\frac{T - T_{amb}}{R_{th}}$ must exist, or the device falls into the thermal runaway state otherwise [6].

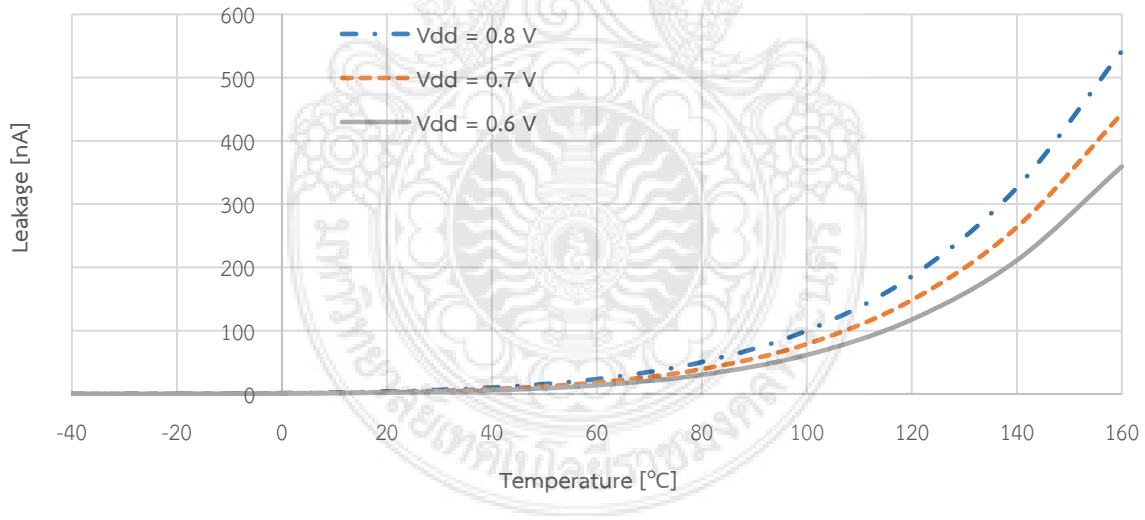


Figure 1. Leakage current vs. temperature for different supply voltage levels in an inverter designed with 14-nm bulk FinFET technology

The first part of $P_{circuit}$ is the static power P_{static} due to subthreshold leakage and gate tunneling leakage. Because of the domination of subthreshold leakage at high temperature, the gate tunneling leakage can be negligible [6]. P_{static} in term of subthreshold leakage is dependent on temperature, supply voltage, and threshold voltage [7], which can be expressed as

$$P_{static} = V_{dd}\left[I_0 e^{q(\frac{V_{gs}-V_{th}}{mk_BT})}(1 - e^{-q(\frac{V_{ds}}{k_BT})})\right] \quad (3)$$

where m is the body-effect coefficient. TEI also raises P_{static} through the decrease in V_{th} providing positive feedback of heat to the device. The total leakage current as a function of temperature in an inverter for different supply voltage levels is illustrated in Figure 1. We can further notice from Figure 1 that V_{dd} variation has small impact on leakage at low temperature. However, V_{dd} significantly affects the dynamic power ($P_{dynamic}$), the other component of $P_{circuit}$, which is given by

$$P_{dynamic} = \alpha C_L V_{dd}^2 f \quad (4)$$

where α is the activity factor of output node, C_L is the switching capacitance, and f is the clock frequency. Because $P_{dynamic}$ in (4) increases quadratically with V_{dd}, the result of temperature in (2) due to this change also affects the leakage in (3) through V_{th} parameter. Unlike P_{static}, $P_{dynamic}$ itself tends to be insensitive to temperature change. In some personal mobile devices, where additional cooling systems are not feasible, DVFS based techniques, which directly control $P_{dynamic}$, have widely been used to stabilize the chip temperature.

2.2 Temperature effect on BTI aging

BTI effect degrades the device delay over a long period of operation. Under NBTI stress, holes from the inversion layer breaks Si-H bonds at the Si/SiO_2 interface of a negatively biased pFinFET generating incomplete Si^+ bonds called the "interface traps". These interface traps cause an increase in the threshold voltage leading to a decrease in driving current. When the pFinFET device receives positive bias, some of the broken hydrogen atoms and molecules near the interface diffuse back and anneal the broken Si^+ bonds. This NBTI state is called the "recovery" phase where the threshold voltage is shifted back. On the other hand, PBTI is the reciprocal effect of NBTI that affects nFinFETs with high-k gate. PBTI is primarily caused by electron trapping into the high-k defects. PBTI degradation strongly relies on the process and quality of the high-k material [8].

The total BTI effects can be described by the Reaction-Diffusion (RD) model. In this work, we use a simplified RD model for long-term threshold voltage shift $\Delta V_{th,BTI}$ [9], [10], which is given by

$$\Delta V_{th,BTI} = \chi \left(\frac{\sqrt{K_s^2 \left(C(T),(V_{gs}-V_{th})\right) st_{cycle}}}{1-K_r^{\left(\frac{1}{2n}\right)}(C(T),t)} \right)^{2n} \tag{5}$$

where χ is the BTI coefficient set to be 1 for NBTI and 0.5 for PBTI, K_s and K_r are parameters of the stress and recovery mechanisms, *s* is the fraction of stress time, *t* is the operating time, t_{cycle} is the stress/recovery cycle time, and *n* is the fitting parameter set to be 1/6 for H_2-based RD model. Both K_s and K_r are functions of the diffusion temperature-dependent coefficient, $C(T) = T_0^{-1} exp\left(\frac{-E_a}{k_B T}\right)$ [11]. K_s also relies on the term $(V_{gs} - V_{th})$ which is related to the inversion charge density. All values of parameters in (5) are adopted from [9] and [12], which are assumed valid

for either planar MOSFETs or FinFETs. The threshold voltage shift from BTI is dependent on temperature, time, bias, and original threshold voltage.

While TEI causes a FinFET design to run faster, BTI aging becomes worse at high temperature. In presence of TEI, the decrease in threshold voltage of the device due to $\Delta V_{th,TEI}$ intensifies $\Delta V_{th,BTI}$ in (5).

2.3 Related works

As power has become a primary concern for modern system-on-chip designs, various works on power/thermal analysis and management have recently been proposed. A TEI-aware DTM technique was introduced in [2] to minimize the power consumption of FinFET based circuits without performance penalty. Reference [13] presents a new thermal simulation approach for FinFET based ICs by using the proper orthogonal decomposition (POD) to reduce the degrees of freedom. A design for thermal performance as well as an effort to predict the thermal time constant of multi-fin FinFETs were introduced in [14]. The work in [15] developed a source-level simulation method to perform a full range of performance, energy, reliability, power, and thermal estimation.

Many studies have investigated impacts of parameter variations on BTI aging, and proposed a large variety of BTI mitigation techniques for FinFET based designs over the past few years. The work in [16] analyzed BTI dependency on supply voltage and design styles for SRAM cells, and compared BTI vulnerability of planar MOSFET and FinFET based designs. In [17], NBTI degradation in datapath logic circuits was evaluated under workload and architectural parameter variations. The work in [18] used high immunity on NBTI of planar devices to develop a NBTI mitigation technique for GPUs by replacing some FinFET devices with planar MOSFETs, and slightly modifying the original GPU architectures. Frequency dependence and delay effect on NBTI was measured in [19]. The study in [20] used the BTI dependency on workload to develop a machine learning-

based monitoring method to estimate aging delay in embedded processers at RTL. However, BTI analyses that take into account thermal/power characteristics in conventional CMOS and FinFET based designs have rarely been reported. An assessment of NBTI in the presence of self-heating in FinFETs at the device level was performed by the work in [4]. In [21], the effect of temperature-induced variability on BTI aging in DVFS designs was examined without TEI consideration. On the other hand, the work in [3] evaluated combined effects of TEI and BTI on performance of FinFET circuits, but temperature dependency on supply voltage and frequency was excluded.

Chapter 3. Research Methodology

This work mainly focuses on developing a trustworthy simulation framework used to investigate the combined effects of TEI, BTI, and temperature on the circuit performance. To begin with, a fine-grained workload/temperature-dependent power model for FinFET circuits is developed based on extensive SPICE and logic simulations. In this model, the chip temperature is evaluated by use of the measured power, thermal resistance and capacitance, and ambient temperature. In addition, we introduce a BTI model, which is strongly dependent on the side effect of temperature change resulted from DVFS and TEI. The change in temperature is considered as the TEI-induced threshold voltage shift, which is subsequently used to estimate the aging delay. The total simulation and analysis framework proposed in this paper is illustrated in Figure 2 and will be discussed in the following subsections.

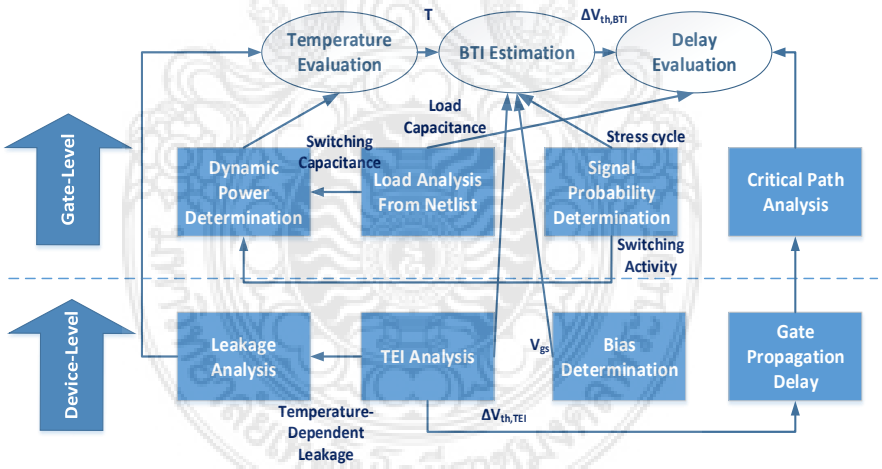
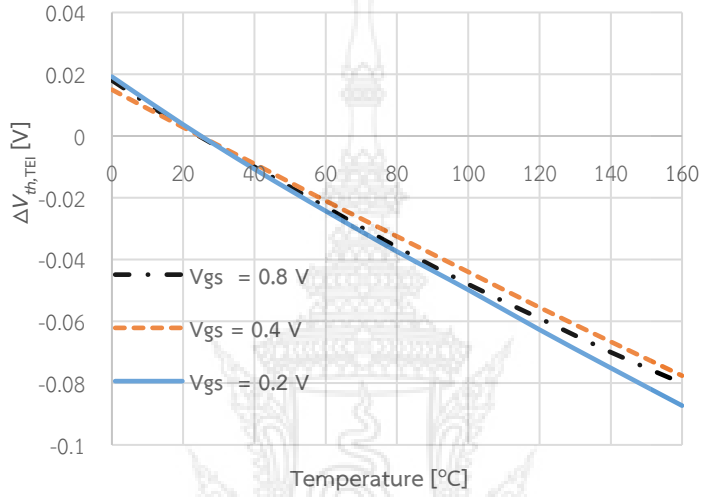


Figure 2. Simulation and analysis framework

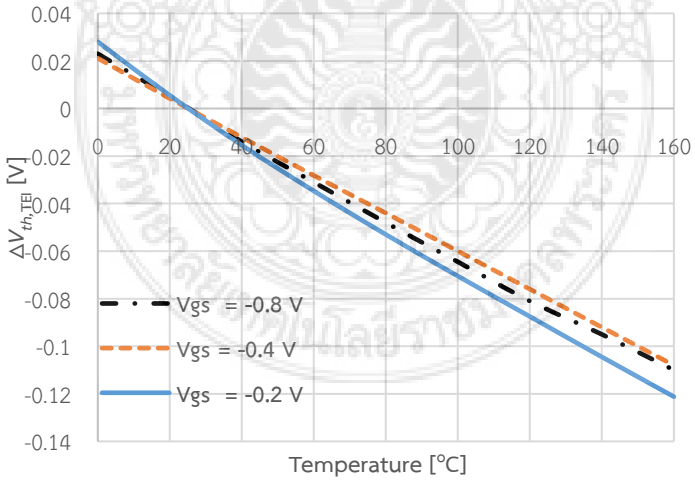
3.1 Temperature evaluation

Our emphasis is placed on design-time analysis of the interrelation among temperature, power, supply voltage, and frequency in a combinational circuit block within a processor at the gate level. To simplify the influence of TEI on performance and degradation mechanisms, SPICE is used

to map I_{on} at any temperature to the change in threshold voltage $\Delta V_{th,TEI}$ providing the same I_{on} at a fixed-nominal temperature level. Figure 3 plots $\Delta V_{th,TEI}$ and temperature in 14-nm bulk tri-gate n/pFinFETs equivalent to the situation that the device temperature varies around T_0 = 25 °C. It can be seen from Figure 3 that TEI causes $\Delta V_{th,TEI}$ to decrease as temperature increases with almost the same rate for all supply voltage levels.



(a)



(b)

Figure 3. The equivalent shift in threshold voltage with temperature in the 14-nm bulk tri-gate nFinFET (a) and pFinFET (b) for different V_{gs}

Table 1. $|V_{gs}|$ of pFinFETs in a 3-Input NOR gates

Input Pattern[a.]			|Vgs| [V] (stress/recovery)[b.]		
x_2	x_1	x_0	M_2	M_1	M_0
0	0	0	0.8 (s1)	0.8 (s1)	0.8 (s1)
0	0	1	0.07 (r)	0.09 (r)	0 (r)
0	1	0	0.07 (r)	0 (r)	0.8 (s1)
0	1	1	0.02 (r)	0 (r)	0 (r)
1	0	0	0 (r)	0.8 (s1)	0.8 (s1)
1	0	1	0 (r)	0.73 (s2)	0 (r)
1	1	0	0 (r)	0 (r)	0.8 (s1)
1	1	1	0 (r)	0 (r)	0 (r)

[a.] The input value of x_n corresponds to the input of transistor M_n.
[b.] pFinFET M_0 is connected to the power supply followed by M_1 and M_2.

The temperature-dependent leakage of all gates in the cell library under TEI can also be evaluated using SPICE. Alternatively, at higher level of the design, we can perform probabilistic logic simulations to obtain the dynamic power consumption defined by switching activities, and to determine the switching capacitance using netlist information. As referred from [3], the dynamic power for each parallel transistor can be estimated based on the fraction of the device switching activity, whereas for each transistor in series, it can be calculated based on the fraction of the device load capacitance. The steady-state circuit temperature can be searched in an iterative manner using the total power and thermal resistance of the circuit. Nevertheless, the thermal resistance, which relies on materials, geometries, and packages of circuits, is difficult to derive analytically. In our simulation, we adopt the thermal resistance of 14-nm FinFETs from [14] and assume that the thermal resistance is inversely proportional to the number of fins [1].

3.2 NBTI evaluation

Initially, we perform an experiment to investigate the combined impact of NBTI and TEI on circuit performance. In this experiment, PSO algorithm is used to construct a long-term NBTI model guided by the dynamic degradation model of NBTI as given in the following equations [22]:

$$\text{Stress: } \Delta V_{th}(t) = \left[K_v (t - t_0)^{\frac{1}{2}} + \sqrt[2n]{\Delta V_{th}(t_0)}\right]^{2n} \tag{6}$$

$$\text{Recovery: } \Delta V_{th}(t) = \Delta V_{th}(t_1)\left(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(t - t_1)}}{2t_{ox} + \sqrt{Ct}}\right) \tag{7}$$

where C is the diffusion temperature-dependent coefficient; n is set to be 1/4 or 1/6 for H diffusion or H_2 diffusion, respectively [23]; the times t_0 and t_1 correspond to the time at the beginning of stress phase and recovery phase, respectively; ξ_1 and ξ_2 are back diffusion constants; t_e is the effective diffusion distance; t_{ox} is the oxide thickness; and the term K_v is given by

$$K_v = \left(\frac{q t_{ox}}{\epsilon_{ox}}\right)^3 {K_1}^2 C_{ox}(V_{gs} - V_{th0})\sqrt{C} exp\left(\frac{2E_{ox}}{E_0}\right) \tag{8}$$

where E_{ox} is the vertical electric field, E_0 is a technology dependent parameter, K_1 is a constant, V_{gs} is the gate-source voltage of the device, and V_{th0} is the original threshold voltage.

PSO is one of the evolutionary computation methods to search for potential solutions based on swarm intelligence of insects, birds, or fish. In PSO, an individual or particle is represented by its position and velocity which indicate a possible solution and search direction, respectively. All particles iteratively evaluate their move and update the position and velocity based on their own and group's (swarm's) experiences. The position and velocity vectors of the i-th particle in the d-dimensional search space are represented as $\mathbf{P_i} = [p_{i,1}, p_{i,2}, p_{i,3}, \ldots, p_{i,d}]^{\top}$ and

$\mathbf{V_i}$ = [$v_{i,1}$, $v_{i,2}$, $v_{i,3}$,..., $v_{i,d}$] $^{\top}$, respectively. Each particle has its own personal best position, $\mathbf{P_i^b}$ = [$p_{i,1}^b$, $p_{i,2}^b$, $p_{i,3}^b$,..., $p_{i,d}^b$] $^{\top}$, achieved at the end of *j*-iteration. In the entire swarm, the best of the personal best position found so far is represented as the global best position, $\mathbf{P^g}$ = [p_1^g, p_2^g, p_3^g,..., p_d^g] $^{\top}$. At the (*j*+1)-iteration, the particle velocity, $\mathbf{V_i^{j+1}}$, and position, $\mathbf{P_i^{j+1}}$, are updated according to the evolution equations [24] as follows.

$$\mathbf{V_i^{j+1}} = \omega * \mathbf{V_i^j} + c_1 * r_1 * \left(\mathbf{P^g} - \mathbf{P_i^j}\right) + c_2 * r_2 * \left(\mathbf{P_i^b} - \mathbf{P_i^j}\right) \quad (9)$$

$$\mathbf{P_i^{j+1}} = \mathbf{P_i^j} + \mathbf{V_i^j} \quad (10)$$

In (9) and (10), **ω** is the inertia weight, c_1 and c_2 are the learning factors, and r_1 and r_2 are random numbers in [0, 1].

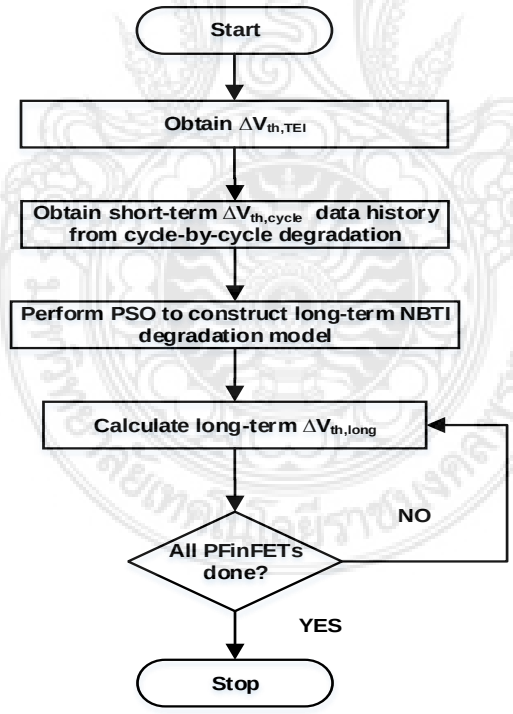


Figure 4. Flowchart of PSO based TEI-aware long-term NBTI prediction

Flowchart of our proposed PSO based long-term NBTI prediction is shown in Figure 4. Since a PFinFET receives arbitrary stress level and time duration, depending on its V_{gs} for each input cycle, the results from the dynamic model are recorded as degradation history that helps capture stress-recovery pattern of the device under actual operation. The long-term NBTI degradation at the time t in a PFinFET can be approximated as the power law degradation:

$$\Delta V_{th,long}(t) = K_c * t^{K_e} \tag{11}$$

where K_c and K_e are constants which are dependent on various operating parameters such as the supply voltage, temperature, probability of stress, input cycle time, and device geometrical parameters.

A nonlinear problem is formulated to fit the input-dependent constants, K_c and K_e, in (11). The objective is to minimize the sum of square error (*SSE*) between the short-term cycle-by-cycle data ($\Delta V_{th,cycle}$) resulted from (6) and (7) and the generated long-term degradation data ($\Delta V_{th,long}$) in (11). The *SSE* can be described as

$$SSE = \sum_{k=1}^{\#of\ data\ points} \left[\Delta V_{th,cycle}(t_k) - \Delta V_{th,long}(t_k)\right]^2 \tag{12}$$

In summary, the nonlinear fitting problem used for constructing the long-term threshold voltage degradation model due to NBTI can be stated as

$$\textbf{Fit: } K_c, K_e$$
$$\textbf{Min: } SSE \tag{13}$$

```
//Initialization
for each particle i = 1 to swarm size do {
   Randomly generate Pi and Vi
   Pib ← Pi
   Save SSE of each Pib
}// end for each particle

Save minimum SSE of the swarm
Pg ← best {Pib, i = 1, … , swarm size}//Pib with minimum SSE

//Main Loop
for each iteration j = 1 to #of max iteration do {

   //Evaluation
   for each particle i = 1 to swarm size do {
        if (SSE of Pi < SSE of Pib) then {
             Pib ← Pi
             Save SSE of current Pib
        }
        if (SSE of Pib < SSE of Pg) then {
             Pg ← Pib
             Save minimum SSE
        }
   }// end for each particle

   //Update
   for each particle i = 1 to swarm size do {
        Vi ← ω*Vi + c1*r1*(Pg − Pi) + c2*r2* (Pib − Pi)
        Pi ← Pi + Vi
        // ω is the inertia weight
        // c1 and c2 are the learning factors
        // r1 and r2 are random numbers in [0, 1]

   }//end for each particle

}//end for each iteration
```

Figure 5. Pseudocode of PSO algorithm for long-term NBTI prediction

Next, we employ PSO to solve the above nonlinear problem. In this study, the generated values for each particle *i*, $K_{c,i}$ and $K_{e,i}$, associated with the fitting constants, K_c and K_e, are

described as the position of a 2-dimensional particle (d = 2), and thus, $\mathbf{P_i} = [K_{c,i}, K_{e,i}]^{\top}$. Figure 5 sketches the pseudocode of PSO algorithm applied to this problem. To begin with, the position and velocity vectors, $\mathbf{P_i}$ and $\mathbf{V_i}$, are initialized with random values. Because there is no previous $\mathbf{P_i}$ value for comparison in this initialization stage, the personal best position of the *i*-th particle, $\mathbf{P_i^b}$, is set to be the same as $\mathbf{P_i}$. In the main loop of PSO algorithm, the current particle position, $\mathbf{P_i}$, is evaluated and compared with the previous personal best position, $\mathbf{P_i^b}$, and the global best position, $\mathbf{P^g}$. If the current $\mathbf{P_i}$ provides smaller *SSE*, it will replace $\mathbf{P_i^b}$ or both $\mathbf{P_i^b}$ and $\mathbf{P^g}$. At the end of the main loop, the particle velocity, $\mathbf{V_i}$, and position, $\mathbf{P_i}$, are updated according to the evolution equations [24], and set to be the velocity and position of the corresponding particle for the next iteration.

3.3 BTI estimation

The proposed BTI (NBTI + PBTI) simulation framework takes into account three important variabilities including workload-dependent stress cycle, temperature change from DVFS, and threshold voltage shift due to TEI. In this study, we comprehensively inspect the difference of BTI stress levels depending upon workload and position of the transistor in a series network. Table 1 shows the HSPICE results of V_{gs} for all input patterns of each pFinFET in a 3-input NOR gate implemented with the 14-nm trigate FinFET technology from [25]. From this device-level simulation, the stack of pFinFET may lead to different stress levels (s1 and s2 for this gate type), but we assume that the device has a single recovery level (r) when $|V_{gs}|$ is relatively small compared to $|V_{th}|$. The threshold voltage shift due to BTI $\Delta V_{th,BTI}$ for different j levels of stress considered in our work is given by

$$\Delta V_{th,BTI} = \sum_{j=1}^{\#\ of\ stress\ levels} \left(\frac{P_{s_j}}{P_{stress}}\right) \Delta V_{th,BTI}\left(C_{eff}(T), (V_{gs,j} - V_{th})_{eff}\right) \quad (14)$$

In (14), P_{s_j} is the probability that the device receives stress level *j*, and P_{on} is the probability that the device turns on, which is the probability that the input is logic "0" for NBTI or "1" for PBTI. These stress-related probabilities can be obtained from the gate-level logic simulation. The term $\Delta V_{th,BTI}$ in (14) is modified from (5) to take into account the change in temperature and TEI-induced threshold voltage shift$\Delta V_{th,TEI,k}$ corresponding to mode *k* of DVFS. Particularly, $\Delta V_{th,BTI}$ is considered as a function of $C_{eff}(T)$ and $(V_{gs,j} - V_{th})_{eff}$, where

$$C_{eff}(T) = \sum_{k=1}^{\#DVFS\ modes} \frac{t_k}{t_{op}} T_0^{-1} exp\left(\frac{-E_a}{k_B T_k}\right) \quad (15)$$

In (15), $\frac{t_k}{t_{op}}$ is the fraction of time t_k that the device works in mode *k* and the total time of operation t_{op}, E_a is the activation energy, T_k is the operating temperature, k_B is the Boltzmann's constant, and T_0 is another constant [11]. The term $(V_{gs,j} - V_{th})_{eff}$ can also be obtained in the same manner where V_{th} is the summation of the original threshold voltage and $\Delta V_{th,TEI,k}$. In this work, we assume that in each mode of operation, the circuit receives the same workload resulting in a constant circuit temperature.

3.4 Delay evaluation

Consider the total threshold voltage variation from TEI and BTI. The change of delay can be expressed in a simplified form of the Elmore delay as follows [26], [27].

$$\Delta t_{d,i} = \frac{\alpha(\Delta V_{th,TEI,i} + \Delta V_{th,BTI,i})}{V_{dd} - V_{th0}} t_{d0,i} \quad (16)$$

where $\Delta t_{d,i}$ is the change in delay corresponding to transistor M_i as a result of the total shift in threshold voltage $\Delta V_{th} = \Delta V_{th,TEI,i} + \Delta V_{th,BTI,i}$, and $t_{d0,i}$ is the load-dependent original delay.

The change in delay $\Delta t_{d,i}$ and the total threshold voltage shift in (16) have a linear relationship under a certain load capacitance. For a parallel network, the maximum change in network delay $\Delta t_{d,par}$ happens when one parallel transistor with the largest threshold voltage degradation turns on, i.e.;

$$\Delta t_{d,par} = C_{par} \cdot t_{d0} \cdot \Delta V_{th,max} \tag{17}$$

where t_{d0} is the original delay and the proportional constant C_{par} can be identified by linear fitting. For a series network, the degradation of all devices influences the network delay change $\Delta t_{d,ser}$, which can be obtained from

$$\Delta t_{d,ser} = \sum_{i=0}^{\#of\ inputs-1} \Delta t_{d,i} \tag{18}$$

$$\text{where } \Delta t_{d,i} = C_{ser} \cdot t_{d0,i} \cdot \Delta V_{th,i} \tag{19}$$

and the constant C_{ser} and $t_{d0,i}$ can be identified by the linear relationship between $\Delta V_{th,i}$ and $\Delta t_{d,i}$.

The gate propagation delay is the average value of the falling and rising propagation delay in (17) and (18). Finally, critical path analysis is carried out to estimate the circuit delay.

Chapter 4. Experimental Results

In this chapter, we used the proposed simulation framework to investigate the combined impacts of TEI and BTI and the thermal effects of voltage and frequency variations. Our experimental circuits were selected from the ISCAS-85/89 (combinational parts) and MCNC benchmark suites, and mapped with the cell library that consists of Inverter, and 2- to 4-input NAND and NOR gates. All experimental circuits were designed with the 14-nm tri-gate bulk FinFET predictive technology from [25]. The signal probability of all primary inputs was assumed equal. We extracted the steady-state operating temperature (T) corresponding to the circuit power consumption ($P_{circuit}$) and ambient temperature (T_{amb}) as discussed in Chapter 3 (3.1), which is an important factor for estimating long-term aging delay due to BTI.

4.1 Combined impacts of NBTI and BTI (PSO approach)

Table 3 records the circuit delay after 10 years of NBTI stress in the experimental circuits under different temperature levels of 35 °C, 75 °C, and 125 °C with different TEI and NBTI analysis scenarios. All delay values are normalized with respect to the baseline delay at 25 °C in the second column of the table. For each temperature, in the first column which contains the normalized delay of the circuits under TEI regardless of aging degradation, it can be seen that the TEI can enhance the delay of all experimental circuits as temperature increases. Under TEI, the delay decreases by 1.3%, 7%, and 15% on average at 35 °C, 75 °C, and 125 °C, respectively. On the other hand, the second column of each temperature, which lists the normalized delay of the circuits under NBTI without TEI consideration, shows that the NBTI worsens the circuit delay as temperature increases. However, the rate of delay degradation due to NBTI with respect to the increase in temperature is relatively small compared to the delay improvement by the TEI. For example, the largest delay degradation under NBTI stress regardless of TEI is around 6% in the

Table 2. 10-year Delay under Temperature Variation

Circuit	Baseline Delay at 25 ^{O}C [ps]	Normalized Delay								
		35 ^{O}C			*75 ^{O}C*			*125 ^{O}C*		
		TEI	*NBTI without TEI*	*NBTI with TEI*	*TEI*	*NBTI without TEI*	*NBTI with TEI*	*TEI*	*NBTI without TEI*	*NBTI with TEI*
C17	10.626	0.9860	1.0198	1.0061	0.9263	1.0338	0.9629	0.8413	1.0567	0.9087
C499	85.410	0.9866	1.0183	1.0052	0.9292	1.0313	0.9632	0.8477	1.0524	0.9100
C880	100.699	0.9864	1.0180	1.0047	0.9283	1.0308	0.9617	0.8458	1.0515	0.9070
C1196	69.510	0.9865	1.0182	1.0050	0.9291	1.0310	0.9627	0.8489	1.0519	0.9092
C1355	97.217	0.9863	1.0189	1.0055	0.9277	1.0322	0.9626	0.8444	1.0540	0.9086
C1908	119.086	0.9867	1.0180	1.0049	0.9298	1.0307	0.9631	0.8490	1.0514	0.9101
C2670	191.638	0.9878	1.0170	1.0051	0.9357	1.0292	0.9672	0.8616	1.0492	0.9194
C5315	171.653	0.9871	1.0182	1.0056	0.9321	1.0310	0.9658	0.8540	1.0520	0.9157
C6288	378.969	0.9865	1.0191	1.0059	0.9291	1.0326	0.9644	0.8473	1.0546	0.9122
C7552	142.340	0.9872	1.0180	1.0055	0.9324	1.0308	0.9658	0.8546	1.0516	0.9158
i5	18.197	0.9859	1.0201	1.0064	0.9259	1.0343	0.9631	0.8405	1.0575	0.9087
i6	202.643	0.9885	1.0165	1.0053	0.9396	1.0281	0.9700	0.8700	1.0471	0.9259
i7	173.813	0.9880	1.0169	1.0052	0.9370	1.0288	0.9683	0.8645	1.0483	0.9219
i8	425.042	0.9848	1.0204	1.0055	0.9198	1.0348	0.9575	0.8274	1.0583	0.8967
i9	235.703	0.9856	1.0212	1.0071	0.9242	1.0361	0.9633	0.8368	1.0605	0.9087
S838	151.903	0.9866	1.0156	1.0024	0.9293	1.0266	0.9580	0.8476	1.0445	0.9005
S5378	77.501	0.9869	1.0172	1.0045	0.9313	1.0294	0.9631	0.8521	1.0493	0.9106
S13207	236.662	0.9877	1.0135	1.0014	0.9350	1.0231	0.9601	0.8602	1.0387	0.9062
S15850	307.890	0.9877	1.0159	1.0038	0.9352	1.0271	0.9646	0.8606	1.0453	0.9145
S35932	154.566	0.9886	1.0164	1.0052	0.9400	1.0279	0.9702	0.8709	1.0468	0.9264
Average		0.9869	1.0209	1.0050	0.9308	1.0305	0.9639	0.8513	1.0511	0.9118

circuit i9 whereas the TEI can improve the performance of this circuit by 16%. The impact of the TEI tends to dominate NBTI effect at high temperature for all of the experimental circuits causing the net delay to decrease.

Under the NBTI stress coupled with the TEI (see the last column of each temperature in Table III), the circuit performance at low temperature slightly degrades due to the domination of the NBTI over the TEI. At 35 °C, the combined effects of NBTI and TEI cause the average delay to increase by 0.5%. On the contrary, at the high temperature of 125 °C, the delay decreases as much as 10% in some circuits under these two phenomena. If we consider the impact of NBTI on the circuits under TEI at a particular temperature by comparing the first and last columns of each temperature in Table III, it can also be noticed that the circuit delay due to NBTI increasingly worsens at high temperature. In the experiment, the performance degraded from the baseline delay at 35 °C, 75 °C, and 125 °C (the first column of each temperature) are 1.8%, 3.5%, and 7.1%, respectively.

In this part of study, the operating temperature is assumed to be constant for each analysis. However, during actual operation, the temperature of a part of the circuit dynamically changes upon the power dissipation, workload patterns, and thermal resistance. A more accurate NBTI prediction requires increasingly complicated thermal/power models to identify the steady-state temperature which affects the degradation and timing performance for different parts of the circuit. Furthermore, future work directions extended from this investigation may include an exploration of other temperature-dependent aging mechanisms that are more severely vulnerable to heat than NBTI.

4.2 Combined impacts of TEI and BTI

This part of the experiment explores the impacts of BTI and TEI in each circuit under test for a nominal set of supply voltage and frequency levels, namely *active mode* (f = 2 GHz and V_{dd} = 0.8 V). The normalized results of BTI-induced delay degradation in Table 2 is evaluated at the operating temperature T, which can be obtained from our proposed thermal model. The values of T are somewhat above T_{amb} = 25 °C depending on $P_{circuit}$ and thermal resistance (R_{th}) of the

experimental circuits. It can be seen from the second column of Table 2 that BTI together with TEI causes all circuits to degrade by 1.7% to 2.7% after 10 years of operation. However, if the circuit performance at T = 25 °C is set to be the baseline level, all experimental circuits at actual operating temperature (which is hotter than the baseline level) gain as large as 6.0% – 7.6% performance improvement from TEI even though BTI still exerts influence over them. In the last column, the increase in power consumption for each circuit is reported with respect to the baseline power at T = 25 °C. It can be clearly seen from these results that the total power of all circuits rises up to 10.7% of the baseline level due to increased leakage.

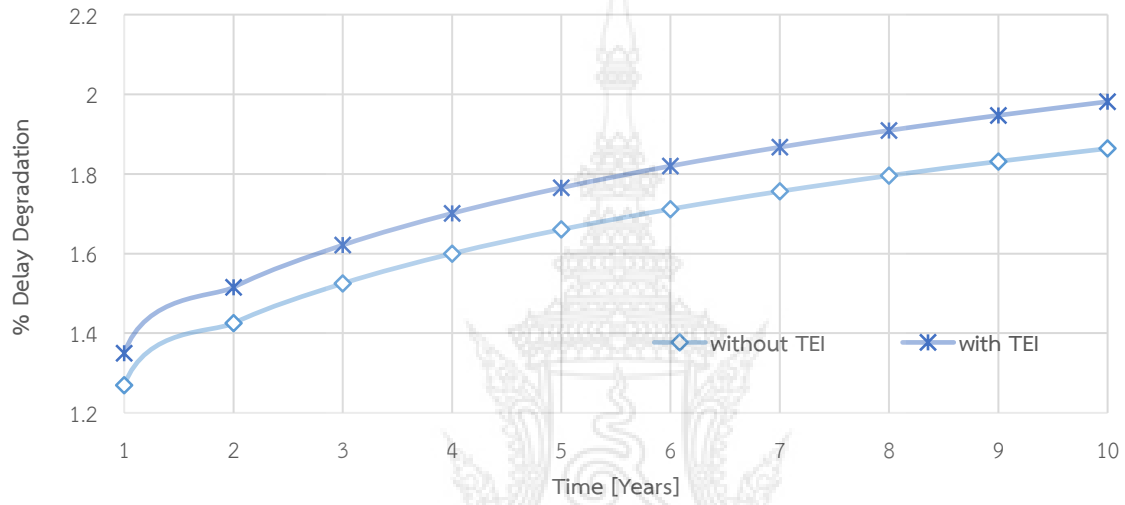
Table 3. Aging degradation, performance, and power under BTI and TEI after 10-year operation

Circuits	BTI Degradation (%)[a.]	Performance Gain (%)[a., b.]	Increased Power (%)[a, b.]
C2670	2.12	6.56	6.31
C6288	2.26	6.87	6.91
C7552	2.23	6.46	6.58
i7	2.00	5.60	10.28
i9	2.74	7.62	10.72
S5378	2.04	6.24	6.04
S15850	1.68	4.97	4.30
S35932	2.13	6.02	6.35

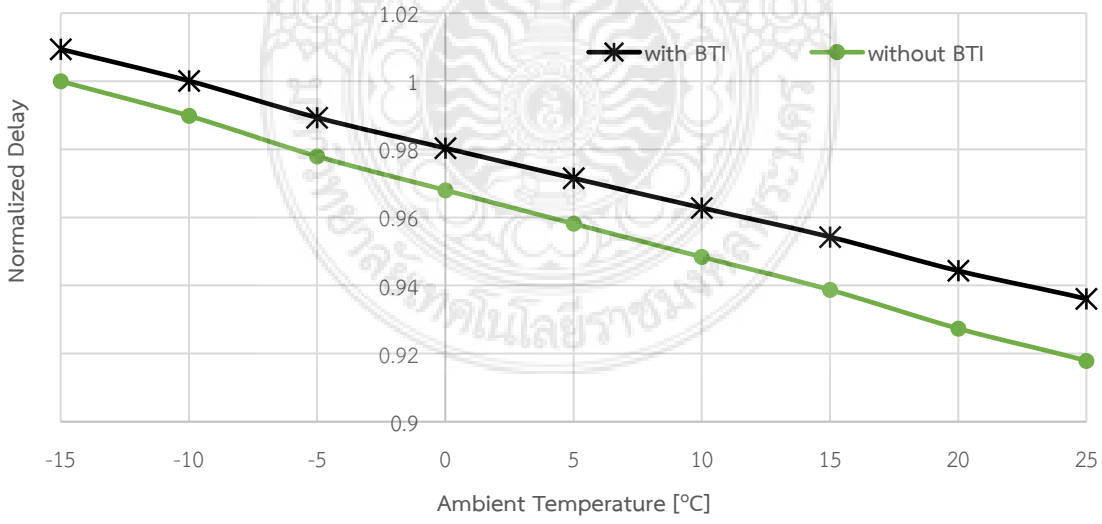
[a.] at the operating temperature T above T_{amb} = 25 °C
[b.] compared to the baseline level at T = 25 °C

Figure 6(a) shows the comparison of long-term delay degradation from BTI-free baseline level at T_{amb} = 25 °C for the circuit C499 when $\Delta V_{th,TEI}$ is considered or not in BTI estimation. From the figure, the conventional BTI prediction approach that does not reckon with TEI provides smaller delay degradation results compared to our approach where heat accumulated from TEI intensifies BTI aging. In Figure 6(b), the normalized circuit delay results are plotted with T_{amb} when

BTI stress over 10 years is either taken into account or not. Besides, the baseline delay is obtained at T_{amb} = -15 °C without BTI stress. It is evident from the figure that TEI enhances the performance of this FinFET benchmark circuit as temperature increases, whereas BTI increasingly worsens the circuit performance at high temperature. However, after 10-year operation, the circuit still runs faster with temperature when both TEI and BTI are addressed together.



(a) BTI degradation over operating time at T_{amb} = 25 °C



(b) TEI-induced performance improvement with temperature

Figure 6. Impacts of BTI and TEI on delay performance of the circuit C499

4.3 Impacts of voltage and frequency

To further investigate the impacts of voltage and frequency variations on BTI aging, the experimental FinFET circuits are now configured with two different operating modes of DVFS, namely *active mode* (the same setting as the previous experiment) and additional *standby mode* (f = 1.24 GHz and V_{dd} = 0.6 V). A set of fractions of time that the circuit operates in either mode has been predefined. Table 3 reports 10-year BTI degradation when the fractions of time r_{active} that the experimental circuits run in the active mode are 0.25, 0.5, and 0.75. We can see that BTI aging results in Table 3 decrease when the circuits have shorter operating time in the active mode. It is important that the effect of temperature is required in BTI aging prediction, otherwise BTI under variations in V_{dd} and frequency without their power/thermal influence is relatively untouched.

Table 4. 10-year delay degradation for different fractions of time that the circuits are in active mode

Circuit	10-year Delay Degradation (%)		
	r_{active} = 0.25	r_{active} = 0.5	r_{active} = 0.75
C2670	1.63	1.81	1.98
C6288	1.76	1.95	2.11
C7552	1.72	1.91	2.08
i7	1.56	1.72	1.87
i9	2.08	2.33	2.54
S5378	1.59	1.76	1.91
S15850	1.36	1.48	1.58
S35932	1.63	1.82	1.98

As we realize that TEI can override BTI and raise the circuit power and performance at high temperature, it is possible to eliminate this excessive gain and achieve power reduction even in the active mode. Given that the baseline operation for all experimental circuits is in the active

mode with T_{amb} = 15 °C, we perform TEI-based supply voltage scaling, which lowers V_{dd} by 0.025-V to deal with the increase in power at higher ambient temperature, while maintaining f at 2 GHz and the delay at the baseline level. Table 4 shows the optimal supply voltage, and the outcomes of power reduction and BTI change from the nominal active mode with T_{amb} = 20, 25, 30, and 35 °C. From Table 4, at higher ambient temperature, TEI allows us to scale down larger amount of supply voltage to bring the performance back to the baseline level, and hence, we achieve larger power reduction (up to 66%). In addition, lowering supply voltage cools down the operating temperature leading to a slight decrease in BTI aging degradation for all circuits.

Table 5. TEI-based supply voltage scaling to reduce power consumption

Circuit	T_{amb} = 20 °C			T_{amb} = 25 °C			T_{amb} = 30 °C			T_{amb} = 35 °C		
	Optimal V_{dd} (V)	*Power Save (%)*	*BTI Change (%)*	*Optimal V_{dd} (V)*	*Power Save (%)*	*BTI Change (%)*	*Optimal V_{dd} (V)*	*Power Save (%)*	*BTI Change (%)*	*Optimal V_{dd} (V)*	*Power Save (%)*	*BTI Change (%)*
C2670	0.775	6.42	-0.06	0.7	24.80	-0.29	0.65	36.00	-0.45	0.6	46.34	-0.62
C6288	0.75	12.91	-0.16	0.7	24.77	-0.30	0.625	41.06	-0.55	0.575	51.26	-0.80
C7552	0.75	12.83	-0.15	0.7	24.89	-0.31	0.625	40.87	-0.50	0.575	51.00	-0.71
i7	0.75	13.29	-0.13	0.675	31.02	-0.30	0.625	42.16	-0.45	0.55	56.48	-0.64
i9	0.775	6.99	-0.12	0.7	26.06	-0.44	0.65	38.04	-0.72	0.575	53.17	-1.05
S5378	0.75	12.59	-0.11	0.7	24.61	-0.26	0.55	54.36	-0.58	0.475	66.45	-0.76
S15850	0.75	12.49	-0.09	0.7	24.03	-0.16	0.6	44.67	-0.33	0.525	57.99	-0.45
S35932	0.775	6.42	-0.05	0.7	24.82	-0.28	0.65	36.03	-0.44	0.6	46.38	-0.60

Chapter 5. Conclusions

This work develops a simulation framework for BTI aging and applies it to FinFET combinational circuits to explore the impacts of temperature, supply voltage, and frequency variations on the circuit performance and reliability. The analysis results reveal that TEI, which improves the timing performance of FinFET devices at high temperature, additionally worsens BTI degradation at a particular operating temperature in all experimental circuits. However, the domination of TEI over BTI still causes all circuits to run faster as temperature increases. BTI degradation is also sensitive to supply voltage and frequency through power and temperature, and thus, the standby mode of DVFS with lower V_{dd} and frequency can moderate BTI aging due to decreased temperature with a loss of performance. Finally, in the active mode of DVFS considering TEI, we introduce a power reduction technique that scales the supply voltage down to reduce larger amount of excessive power induced by TEI for circuits running at higher ambient temperature. The proposed approach accomplishes power reduction as large as 66% and slight decrease in BTI degradation in some hot circuits while maintaining the performance at a given cooler baseline level with maximum frequency.

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Appendix: Researcher Short Biographies

1. WARIN SOOTKANEUNG, Ph.D. (principal investigator)

Office: Department of Computer Engineering, Faculty of Engineering
Rajamangala University of Technology Phra Nakhon (RMUTP)

Cell Phone: (+66) 83-029-2275

Email: warin.s@rmutp.ac.th

Education:

August 2012 Ph.D. (computer engineering)
Dissertation: "*Reliability Improvement against Soft Errors in Nanometer Digital Circuits*"
From: University of Wisconsin-Madison, USA.

May 2009 M.S. in Electrical Engineering (computer engineering)
From: University of Wisconsin-Madison, USA.

August 2003 M.Eng. in Electronics Engineering
Thesis: "*The Implementation of Bit-Parallel 5th Order Lattice Wave Digital Filters using FPGA*"
From: King Mongkut's Institute of Technology Ladkrabang, Thailand

May 1998 B.Eng. in Electrical Engineering (with double majors: power engineering and telecommunication engineering)

Senior project: "*The Design of Digital Storage Oscilloscope Interface Card*"

From: Chiang Mai University, Thailand

Work experiences:

January 2012 – May 2012 Teaching Assistant for Digital Engineering Laboratory, Department of Electrical and Computer Engineering (ECE), University of Wisconsin-Madison

March 2004 – August 2006 Associate Director, RMUTP's Radio Station

June 2002– August 2006 Head, Department of Electrical Engineering, Faculty of Technical Education, RMUTP

August 1998 – present Lecturer, Faculty of Engineering, RMUTP

Professional Licenses: Licenses for practicing controlled engineering professions

- Associate Electrical Engineer (Power)
- Associate Electrical Engineer (Telecommunication/Electronics)

Volunteer:

- Thai classical music trainer

- Member of Graduate Student Council, ECE, University of Wisconsin-Madison (November 2010 – August 2012)
- Academic paper reviewer for
    - IEEE Transactions on Computers (TC)
    - Journal of Electronic Testing (JETTA)
    - IEEE International Symposium on Circuits & Systems (ISCAS)
    - Asian Test Symposium (ATS)
    - VLSI Design Conference (VLSID)
- Member of technical program committees for numerous national and international academic conferences.

Research Area:

- Soft error mitigation
- Low power design
- Design for reliability
- VLSI design

Teaching:

- Computer architecture
- Digital system and processor design
- Electric circuit analysis
- Fault-tolerant systems
- Electrical engineering mathematics

Selected Publications:

1. W. Sootkaneung, "The Design of Bit-Serial Lattice Wave Digital Filter Using FPGA," *in Proceedings of the 5th International Conference on Information, Communication, and Signal Processing (ICICS),* Bangkok, Thailand, 2005, pp.559-563.
2. K. K. Saluja, S. Vijayakumar, W. Sootkaneung, X. Yang, "NBTI Degradation: A Problem or a Scare?," *in Proceedings of the 21st International Conference on VLSI Design,* Hyderabad, India, 2008, pp.137-142.
3. W. Sootkaneung and K. K. Saluja, "Sizing Techniques for Improving Soft Error Immunity in Digital Circuits," *in Proceedings of the International Conference on VLSI Design and Communication Systems (ICVLSICOM '10),* Chennai, India, 2010, pp.87-92.
4. W. Sootkaneung and K. K. Saluja, "Gate Input Reconfiguration for Combating Soft Errors in Combinational Circuits," *in Proceedings of the International Conference on Dependable Systems and Networks Workshops (DSN-W 2010),* Chicago, IL, 2010, pp. 107-112.
5. W. Sootkaneung and K. K. Saluja, "Optimizing Device Size for Soft Error Resilience in Sub-Micron Logic Circuits," *in Proceedings of the 2nd Asia Symposium on Quality Electronic Design (ASQED 2010),* Penang, Malaysia, 2010, pp. 235-242.
6. W. Sootkaneung and K. K. Saluja, "On Techniques for Handling Soft Errors in Digital Circuits," *in Proceedings of the International Test Conference (ITC 2010),* Austin, TX, 2010, pp. 1-9: Paper 25.2.
7. W. Sootkaneung and K. K. Saluja, "Soft Error Reduction through Gate Input Dependent Weighted Sizing in Combinational Circuits," *in Proceedings of the 12th International Symposium on Quality Electronic Design (ISQED 2011),* Santa Clara, CA, 2011, pp. 603-610.
8. W. Sootkaneung and K. K. Saluja, "Impact of Body Bias Based Leakage Power Reduction on Soft Error Rate," *in Proceedings of the 25th International Conference on VLSI Design,* Hyderabad, India, 2012, pp. 74-79**.**
9. W. Sootkaneung and K. K. Saluja, "Flip-Flop Selection and Gate Sizing to Reduce Re-Execution Penalty Due to Soft Error," *RMUTP Research Journal,* vol. special issue, pp. 29-42, 2014.

10. S. Chookaew, S. Howimanporn, W. Sootkaneung, W. Pradubsri, P. Yoothai, “Computer Assisted Learning Based on ADDIE Instructional Development Model for Visual Impaired Students,” *in Proceedings of the 22nd International Conference on Computers in Education (ICCE)*, Nara, Japan, 2014, pp. 349-354.
11. S. Chookaew, S. Howimanporn, W. Sootkaneung, V. Hamtanon, S. Chareonthammarong, and N. Chadlee, "A Virtual Zoo-based Learning Approach to Improving Students’ Learning Performance and Attitudes in Chinese Language Course," in Proceedings of the 23rd International Conference on Computers in Education (ICCE), Hangzhou, China, 2015, pp. 575-579.
12. W. Sootkaneung, P. Lapamonpinyo, S. Chookaew, and S. Howimanporn, "NBTI in FinFET Circuits Under the Temperature Effect Inversion," in Proceedings of the 19th IEEE International Conference on Computational Science and Engineering, Paris, France, 2016, pp. 343-350.
13. W. Sootkaneung, S. Chookaew, and S. Howimanporn, "Combined Impact of BTI and Temperature Effect Inversion on Circuit Performance," in Proceedings of the 25th IEEE Asian Test Symposium (ATS), Hiroshima, Japan, 2016, pp. 310-315.
14. S. Howimanporn, S. Tanok, S. Chookaew, and W. Sootkaneung, "Design and Implementation of PSO Based LQR Control for Inverted Pendulum System Using PLC," in Proceedings of the IEEE/SICE International Symposium on System Integration (SII), Sapporo, Japan, 2016, pp. 664-669.
15. S. Howimanporn, S. Tanok, S. Chookaew, and W. Sootkaneung, "Speed Control Technique for Conveyor Using PSO Based PID with Programmable Logic Controller," in Proceedings of the IEEE/SICE International Symposium on System Integration (SII), Sapporo, Japan, 2016, pp. 670-675.

16. W. Sootkaneung, S. Howimanporn, and S. Chookaew, “Soft Error-Aware Leakage Reduction through Body Bias,” RMUTP Research Journal, vol. 11, no. 1, pp. 65-77, January-June 2017.

17. W. Sootkaneung, S. Howimanporn, and S. Chookaew, “Particle Swarm Optimization Based NBTI Modeling for FinFET Circuits,” RMUTP Research Journal, vol. 11, no. 1, pp. 78-91, January-June 2017.

2. SUPPACHAI HOWIMANPORN, D.Eng.

Current Position: Assistant Professor

Office: Faculty of Technical Education, King Mongkut's University of Technology, North Bangkok

Cell Phone: (+66) 089-018-4049

E-mail: suppachai.h@fte.kmutnb.ac.th

Education:

2014	D.Eng. (Mechatronics)
	Asian Institute of Technology
2004	M.Eng. (Control Engineering)
	King Mongkut's Institute of Technology Ladkrabang
1999	B.Eng. (Electrical Engineering)
	King Mongkut's Institute of Technology Ladkrabang

Research Interests:

Measurement and Instrument of automatic control systems, Electrical energy conversion, Power electronics, and PLC control

Selected Publications:

1. ศุภชัย หอวิมานพร และชนินทร์ บุญลักษณานุสรณ์ “การศึกษาเปรียบเทียบวงจรฟลายแบคคอนเวอร์เตอร์ในโหมดการนำกระแสแบบต่อเนื่อง (CCM) และแบบไม่ต่อเนื่อง (DCM)”, *วิศวสารลาดกระบัง* ปีที่ 20 ฉบับที่ 1 หน้า 19-24.

2. ศุภชัย หอวิมานพร และชนินทร์ บุญลักษณานุสรณ์ “การเปรียบเทียบสมรรถนะของวงจรฟลายแบคคอนเวอร์เตอร์ในโหมดการนำกระแสแบบต่อเนื่อง (CCM) และแบบไม่ต่อเนื่อง (DCM)”, *การประชุมวิชาการวิศวกรรมไฟฟ้าครั้งที่ 26* หน้า 764-769.

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4. S. Horwimanporn, C. Silawatchananai, M. Parnichkun, and C. Wuthishuwong, “Double Loop Controller Design for the Vehicle's Heading Control,” in *Proceedings of the 2009 international conference on Robotics and biomimetics*, 2009, pp. 989-994.

5. R. Manasoontorn and S. Howimanporn, “Comparison of Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) in Omni Wheel Robot Power Supply,” in *Proceedings of the 2nd RMUTP International Conference*, 2010, pp. 189-194.

6. S. Wiriya, N. Distaklu, and S. Howimanporn, “Speed Control System Design in Bicycle Robot by Low Power Method,” in *Proceedings of the 2nd RMUTP International Conference*, 2010, pp. 195-201.

7. ศุภชัย หอวิมานพร และ กฤษณ์ เจ็ดวรรณะ “การควบคุมความเร็วมอเตอร์แบบฟัซซีร่วมกับพีไอดี, *การประชุมวิชาการมหาวิทยาลัยเทคโนโลยีราชมงคลครั้งที่ 3*, 2010.

8. จักรพันธ์ แสงสุวรรณ และ ศุภชัย หอวิมานพร “การวัดค่าการกัดกร่อนสนิมเหล็ก ในโครงสร้างคอนกรีตเสริมเหล็กแบบโพลาไรเซชั่น, *การประชุมวิชาการมหาวิทยาลัยเทคโนโลยีราชมงคลครั้งที่ 3*, 2010

9. H. Suppachai and P. Manukid, “Performance Comparison of Balancing Control of an X-Y Planar Inverted Pendulum System by PID, LQR and SMC,” *การประชุมวิชาการทางเทคโนโลยีอุตสาหกรรมและหุ่นยนต์*, 2011

10. H. Suppachai and P. Manukid, “Control of an X-Y Planar Inverted Pendulum Using PSO Based SMC,” *International Journal of Robotics and Automation*, 2014. (In press)

11. S. Chookaew, S. Howimanporn, W. Sootkaneung, W. Pradubsri, P. Yoothai, “Computer Assisted Learning Based on ADDIE Instructional Development Model for Visual Impaired Students,” in *Proceedings of the 22nd International Conference on Computers in Education (ICCE)*, Nara, Japan, 2014, pp. 349-354.

12. S. Chookaew, S. Howimanporn, W. Sootkaneung, V. Hamtanon, S. Chareonthammarong, and N. Chadlee, "A Virtual Zoo-based Learning Approach to Improving Students’ Learning Performance and Attitudes in Chinese Language Course," in Proceedings of the 23rd International Conference on Computers in Education (ICCE), Hangzhou, China, 2015, pp. 575-579.

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14. W. Sootkaneung, S. Chookaew, and S. Howimanporn, "Combined Impact of BTI and Temperature Effect Inversion on Circuit Performance," in Proceedings of the 25th IEEE Asian Test Symposium (ATS), Hiroshima, Japan, 2016, pp. 310-315.

15. S. Howimanporn, S. Tanok, S. Chookaew, and W. Sootkaneung, "Design and Implementation of PSO Based LQR Control for Inverted Pendulum System Using PLC," in Proceedings of the IEEE/SICE International Symposium on System Integration (SII), Sapporo, Japan, 2016, pp. 664-669.

16. S. Howimanporn, S. Tanok, S. Chookaew, and W. Sootkaneung, "Speed Control Technique for Conveyor Using PSO Based PID with Programmable Logic Controller," in Proceedings of the IEEE/SICE International Symposium on System Integration (SII), Sapporo, Japan, 2016, pp. 670-675.

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3. SASITHORN CHOOKEAW, Ph.D.

Current Position: Lecturer

Office: Faculty of Technical Education, King Mongkut's University of Technology, North Bangkok

E-mail: sasithorn.c@.kmutnb.ac.th

Education:

2015	Ph.D. in science and technology education Mahidol University
2007	M.S in computer and information technology King Mongkut's University of Technology Thonburi
2004	B.S. Tech. Ed. in technology education King Mongkut's University of Technology Thonburi

Research interests:

Computer animation and computer aided instruction

Selected publications:

1. M. Pornphisud, **C. Sasithorn** and S. Sunisa, "I POD-BASED Learning System on "ADVERTISING DESIGN" for Communication Art-Digital Media Students at Siam Technology College," *International e-Learning Conference* 2008.

2**. Sasithorn Chookaew**, Kanyupa Jittiwadhna and Parames Laosinhai, "Using an Animated Cartoon Analogy for Enhancing Undergraduate Computer Students' Understanding of Process Management in Operating System," *the Second Annual International Research Conference on Social Sciences and Humanities*, 2009.

3. Dechawut Wanichsan, Patcharin Panjaburee, Parames Laosinchai, Wannapong Triampo, and **Sasithorn Chookaew**, "A majority-Density Approach to Developing Testing and Diagnostic Systems with the Cooperation of Multiple Experts Based on an Enhanced Concept-Effect Relationship Model," *Expert Syst. Appl.*, pp.8380-8388, 2012.

4. **S. Chookaew**, S. Howimanporn, W. Sootkaneung, W. Pradubsri, P. Yoothai, "Computer Assisted Learning Based on ADDIE Instructional Development Model for Visual Impaired Students," *in Proceedings of the 22nd International Conference on Computers in Education (ICCE)*, Nara, Japan, 2014, pp. 349-354.

5. S. Chookaew, S. Howimanporn, W. Sootkaneung, V. Hamtanon, S. Chareonthammarong, and N. Chadlee, "A Virtual Zoo-based Learning Approach to Improving Students' Learning Performance and Attitudes in Chinese Language Course," in Proceedings of the 23rd International Conference on Computers in Education (ICCE), Hangzhou, China, 2015, pp. 575-579.

6. W. Sootkaneung, P. Lapamonpinyo, S. Chookaew, and S. Howimanporn, "NBTI in FinFET Circuits Under the Temperature Effect Inversion," in Proceedings of the 19th IEEE International Conference on Computational Science and Engineering, Paris, France, 2016, pp. 343-350.

7. W. Sootkaneung, S. Chookaew, and S. Howimanporn, "Combined Impact of BTI and Temperature Effect Inversion on Circuit Performance," in Proceedings of the 25th IEEE Asian Test Symposium (ATS), Hiroshima, Japan, 2016, pp. 310-315.

8. S. Howimanporn, S. Tanok, S. Chookaew, and W. Sootkaneung, "Design and Implementation of PSO Based LQR Control for Inverted Pendulum System Using PLC," in Proceedings of the IEEE/SICE International Symposium on System Integration (SII), Sapporo, Japan, 2016, pp. 664-669.

9. S. Howimanporn, S. Tanok, S. Chookaew, and W. Sootkaneung, "Speed Control Technique for Conveyor Using PSO Based PID with Programmable Logic Controller," in Proceedings of the IEEE/SICE International Symposium on System Integration (SII), Sapporo, Japan, 2016, pp. 670-675.

10. W. Sootkaneung, S. Howimanporn, and S. Chookaew, “Soft Error-Aware Leakage Reduction through Body Bias,” RMUTP Research Journal, vol. 11, no. 1, pp. 65-77, January-June 2017.

11. W. Sootkaneung, S. Howimanporn, and S. Chookaew, “Particle Swarm Optimization Based NBTI Modeling for FinFET Circuits,” RMUTP Research Journal, vol. 11, no. 1, pp. 78-91, January-June 2017.